N. Wyrsch

Thin-film transistors (TFT) and flat panel displays (FPD)

Content

- Applications
- History
- Display technologies
- Thin-film transistors
- a-Si:H design and operations
- Issues and research directions

Applications of TFT

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- Flat panel displays
- Flat panel imagers
- Bio-MEMS (DNA chips)
- Chemical sensors
- ….

History of TFT

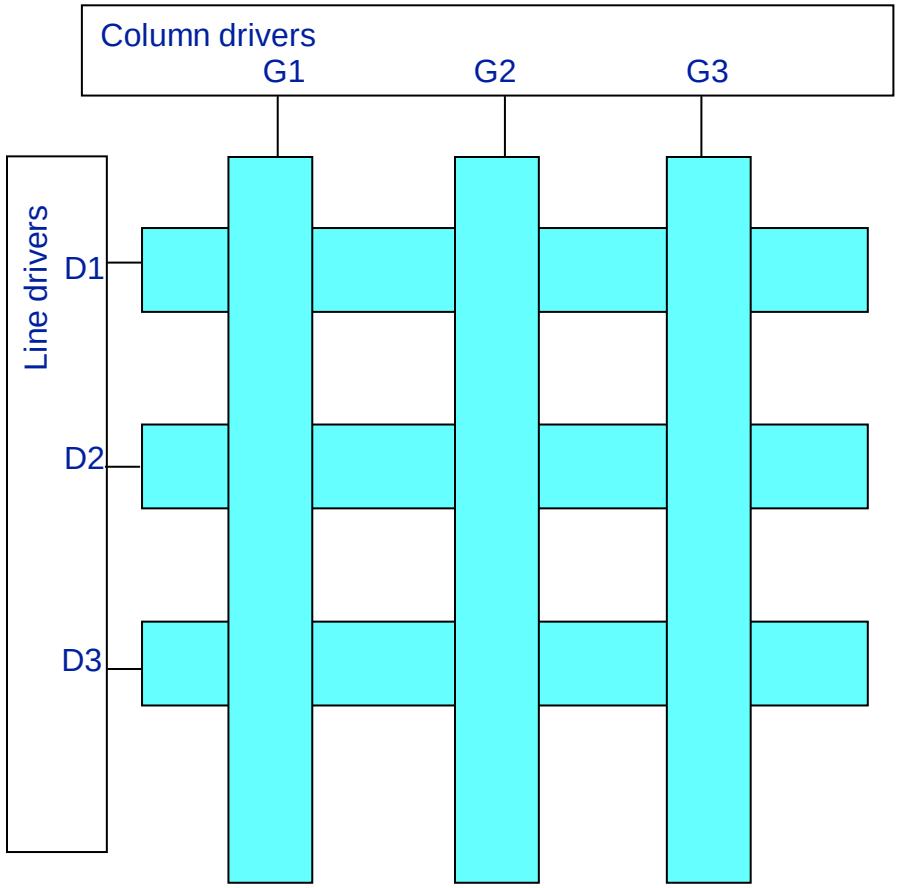
- 1962: First functional TFTs reported by P.K. Weimer using microcrystalline cadmium sulfide (CdS)
- 60's: TFTs in competition with single-crystal silicon MOSFETs for display and electronic applications. Development of the MOSFET limited the field of application of TFTs to display.
- 1973: First active-matrix liquid crystal display (AMLCD) by Brody et al. using CdS
- Late 70's-early 80's, several examples of TFTs were developed from various other materials, e.g CdSe, Te, InSb, Ge; CdS best candidate but without much industrial success
- 1979: First a-Si:H TFT by Spear and Lecomber
- Late 80's: First mass production of a-Si:H based AMLCDs, abandon of CdS
- Today:
  - AMLCD is a market worth tens of billions of € per year
  - a-Si:H is the dominating technology for large FPD
  - Low-temperature poly-silicon (LTPS) or metal-oxide semiconductors used for "special" FPD
  - organic semiconductors being investigated for very low cost displays
  - New applications for TFTs

Display technologies

- Active / passive matrix
- Passive matrix (PM)
  - Liquid crystal display (LCD)
  - Organic light emitting diode (OLED) display
  - Plasma display panel (PDP)
  - Field emission display (FED)
  - Surface conduction electron emission display (SED)
- Active matrix (AM)
  - AM LCD (AMLCD)
  - AM OLED display (AMOLED)
  - Electroluminescent display (ELD)
  - Quantum dot LED display (QDLED, QLED)
  - Electrophoretic display (EPD)

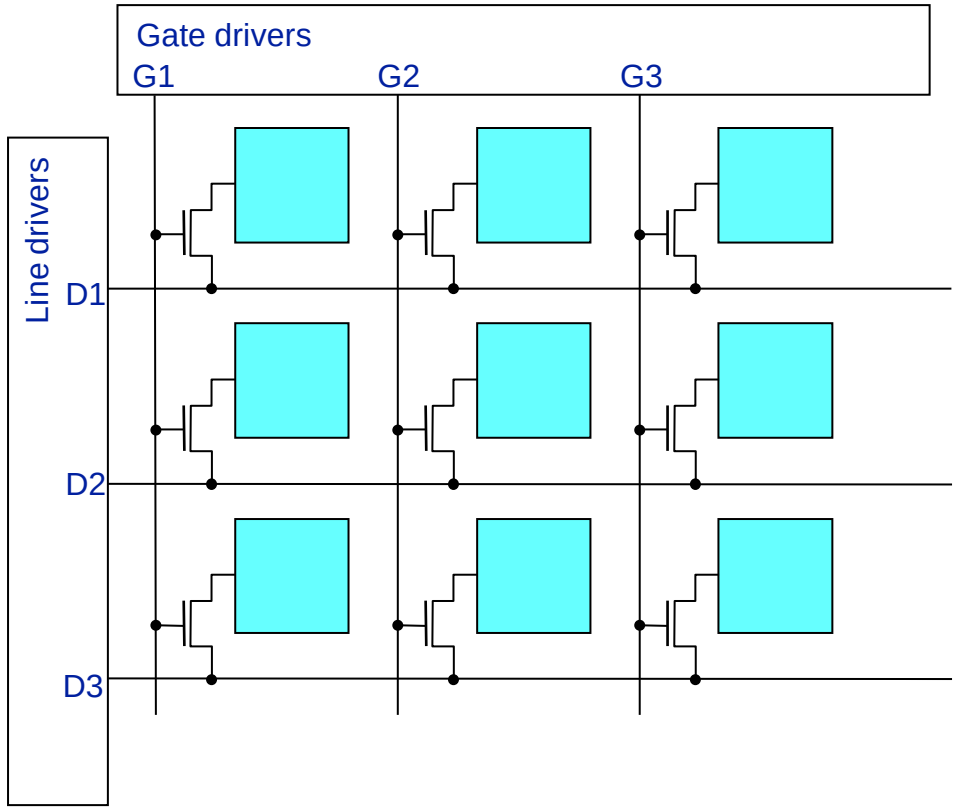
Matrix types

Passive matrix



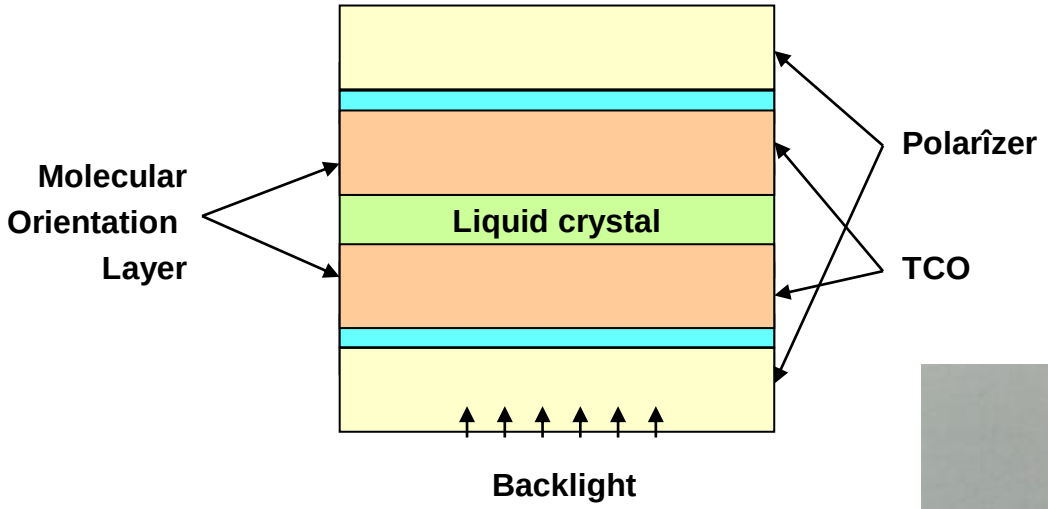
- Pulsed operation

Active matrix



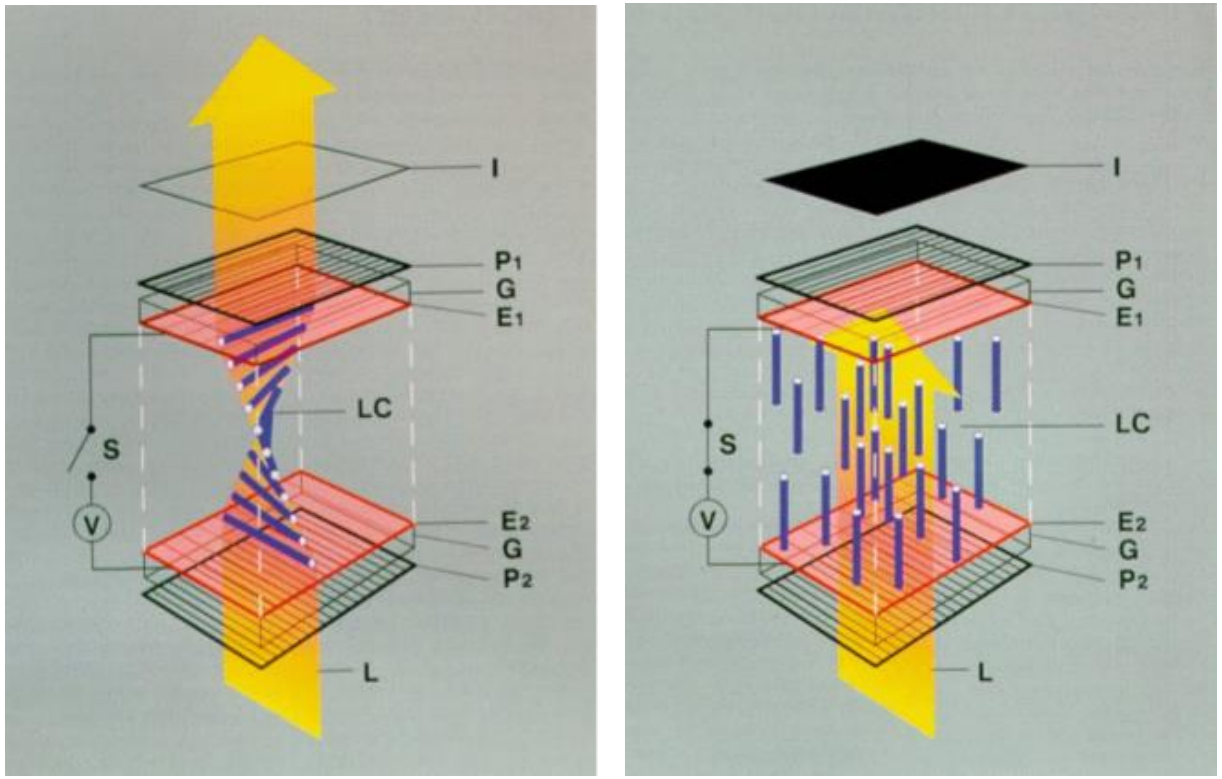
- Continuous operation
- Programming at pixel level

LCD



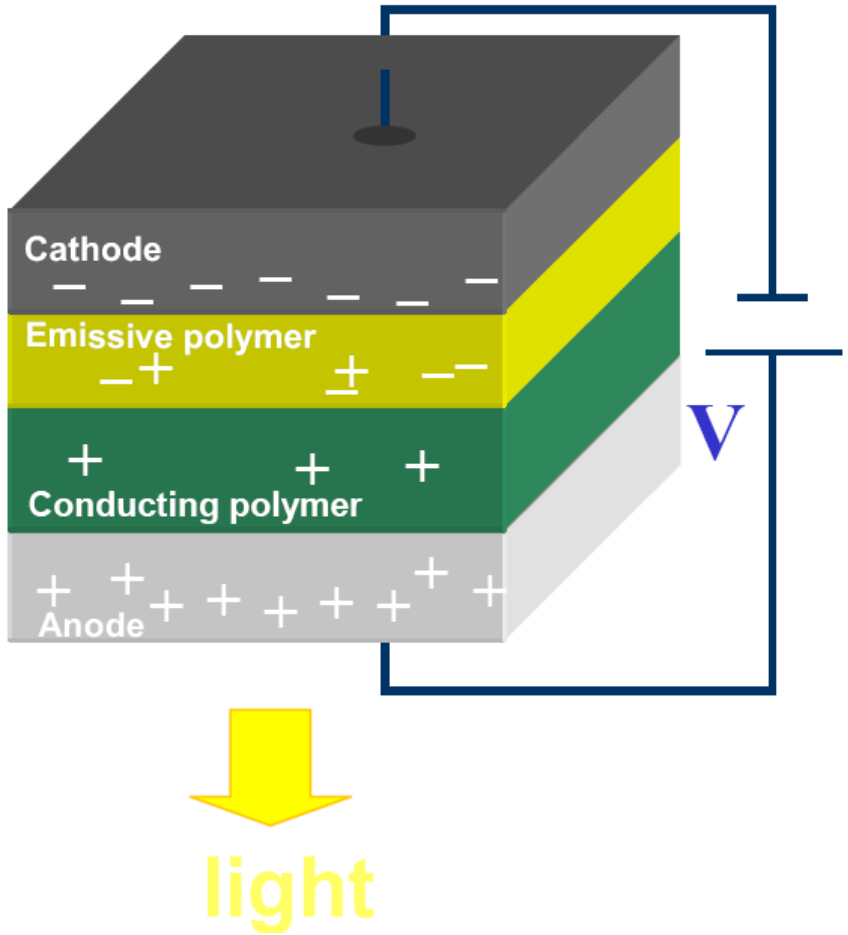
- Light polarization changed by LC in OFF-state)
  → light going through tpixel
- Light polarization unchanged in ON-state)
  → light blocked by second polarizer
- Voltage driven
- Low consumption
- Flexible display possible

Twisted nematic display



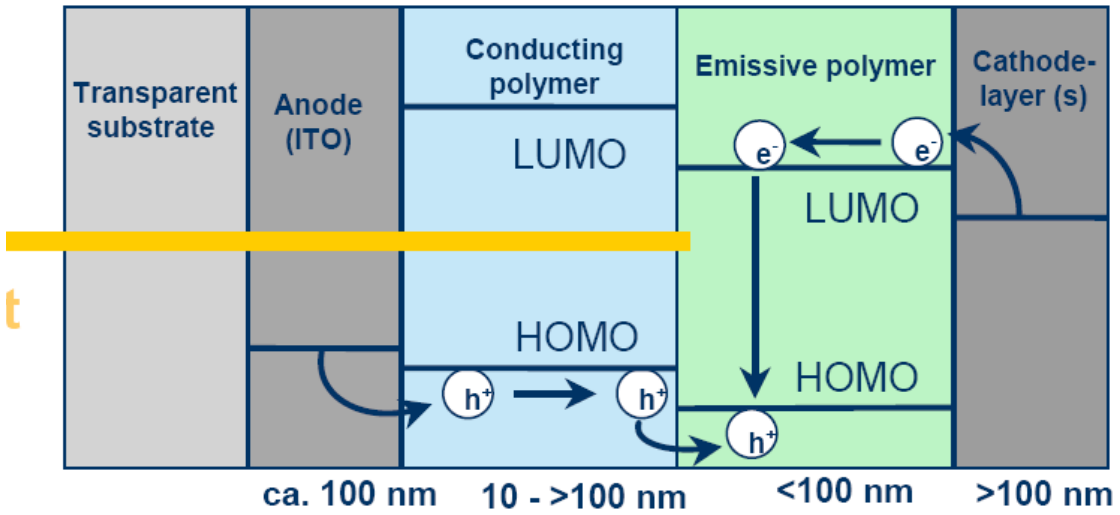
Wikipedia

OLED

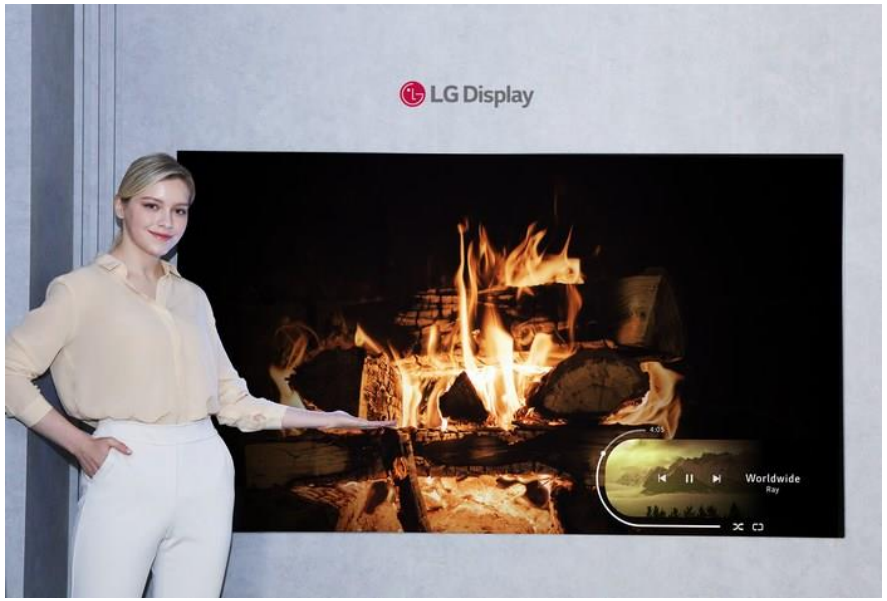


- Organic materials (polymers or small molecules)
- Electrons injected from cathode
- Holes injected from anode
- Radiative recombination of electron hole pairs in the emissive polymer
- Current driven

Energy Level with polymers



OLED displays



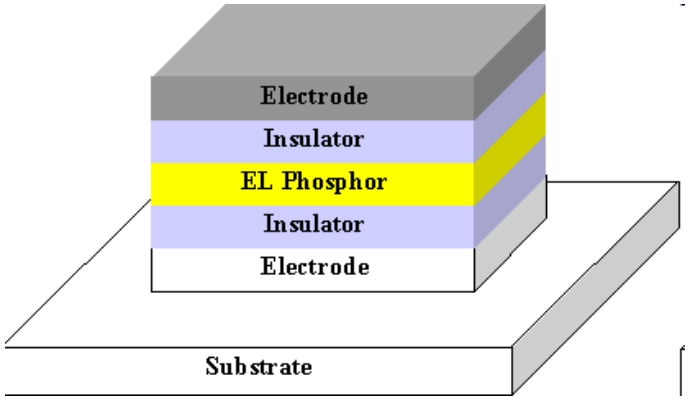
77" OLED transparent and flexible display, LG display

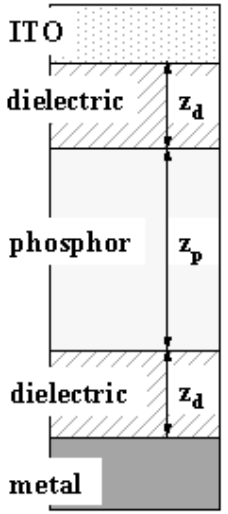
LG

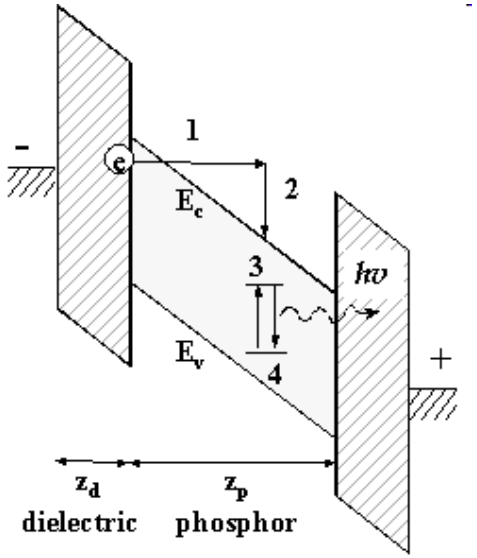
LG display

- Flexible display are coming on the market (foldable and curved displays)
- Large-area displays (>55”) are getting affordable

ELD

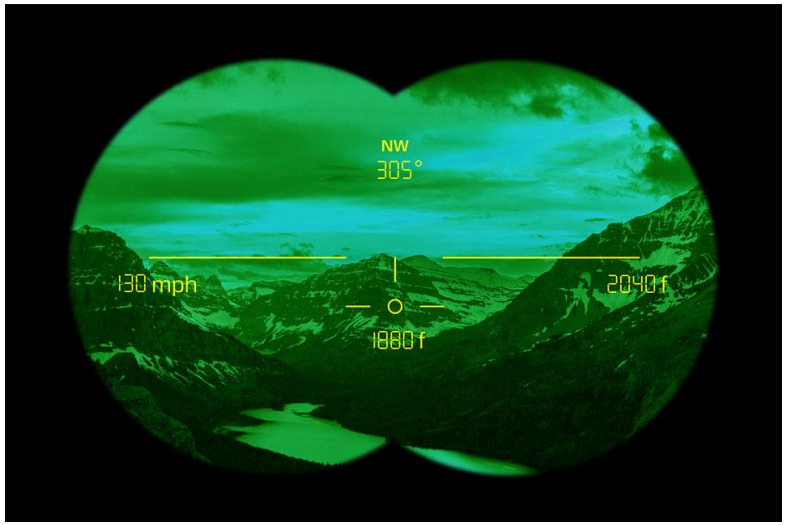






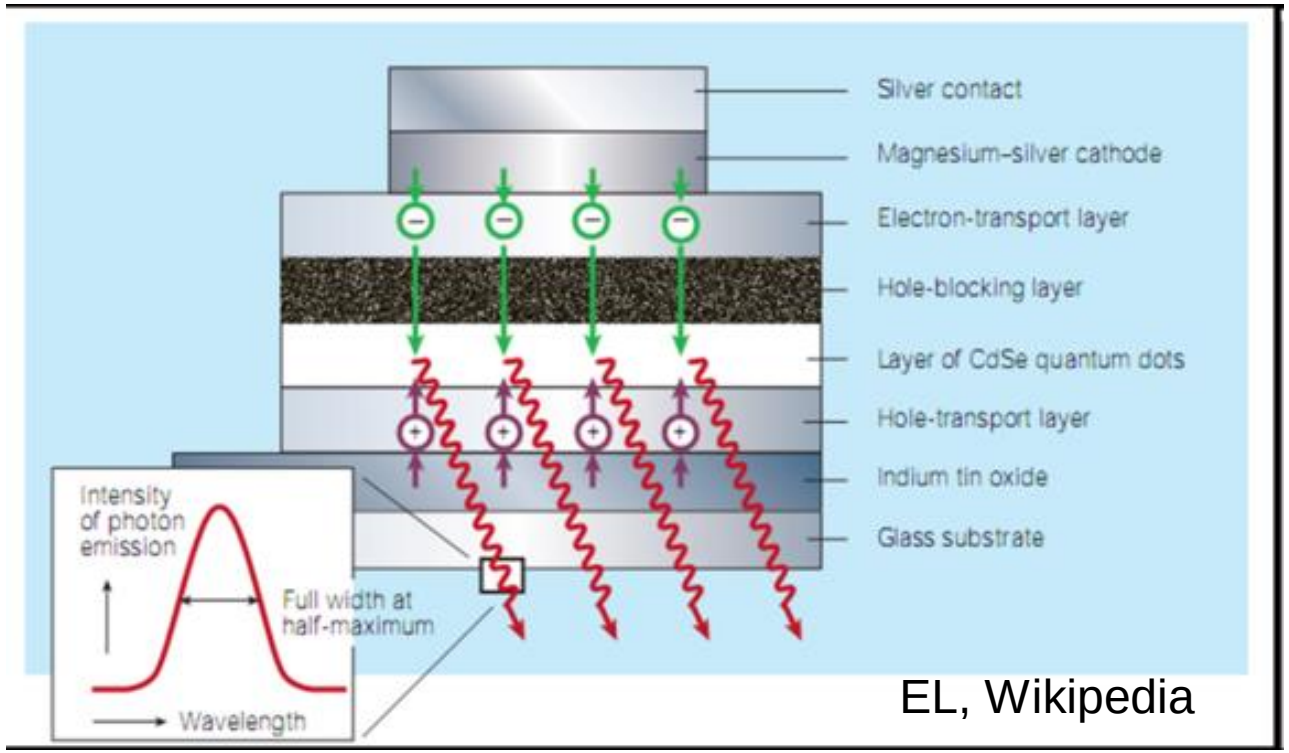
- Very similar to AMOLED with organic or inorganic phosphor
- Commercial products for monochrome display for harsh temperature conditions or transparent displays
- Flexible display possible

https://www.lumineq.com



http://display-innovations.com

QDLED or QLED



EL, Wikipedia

75" Samsung QLED display
Photo-emissive (PL)

- Photoluminescent (PL) or electroluminsent (EL)
- PL displays similar to OLED, EL similar to ELD
- Organic or inorganic (for better lifetime)
- Very narrow emission spectra
- PL in production, EL production to start

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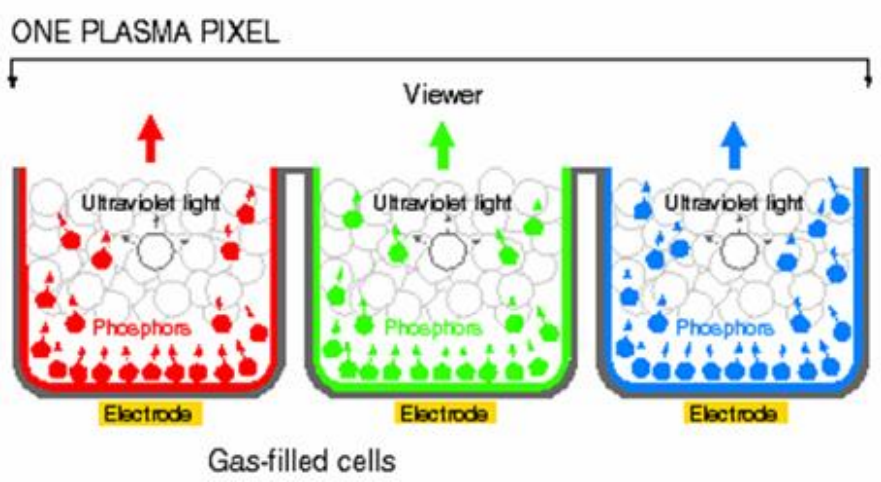
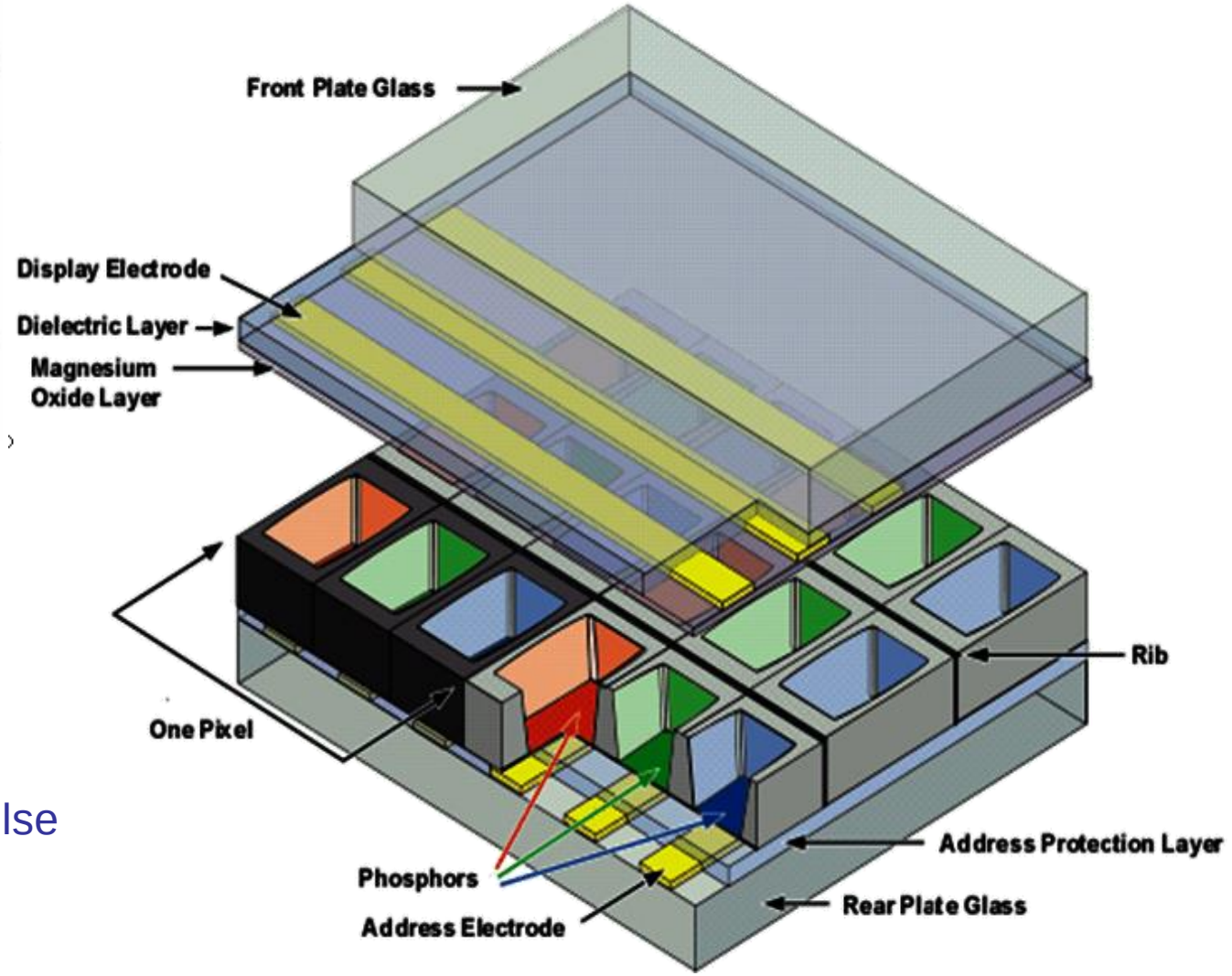
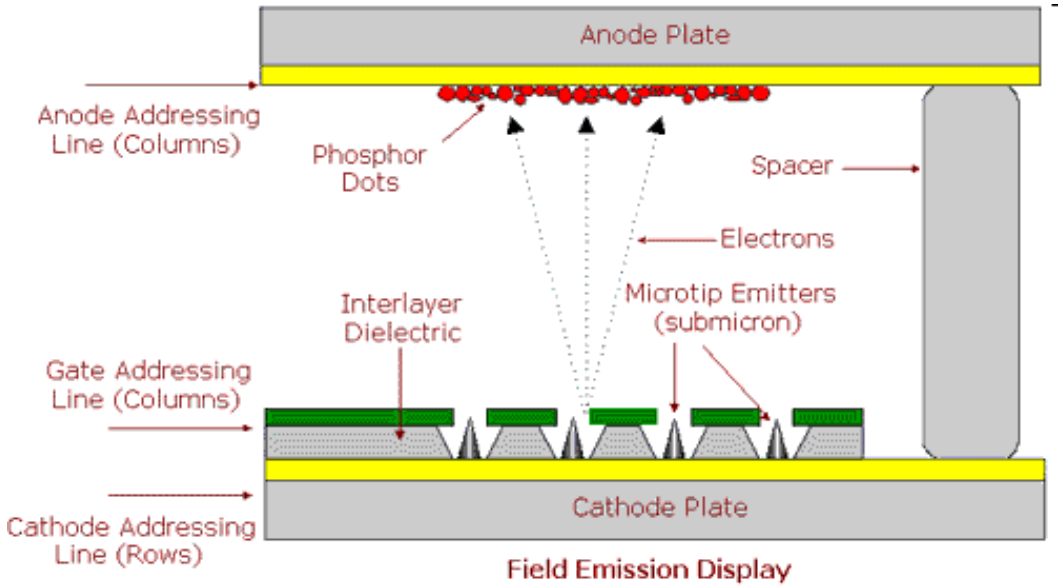
PDP



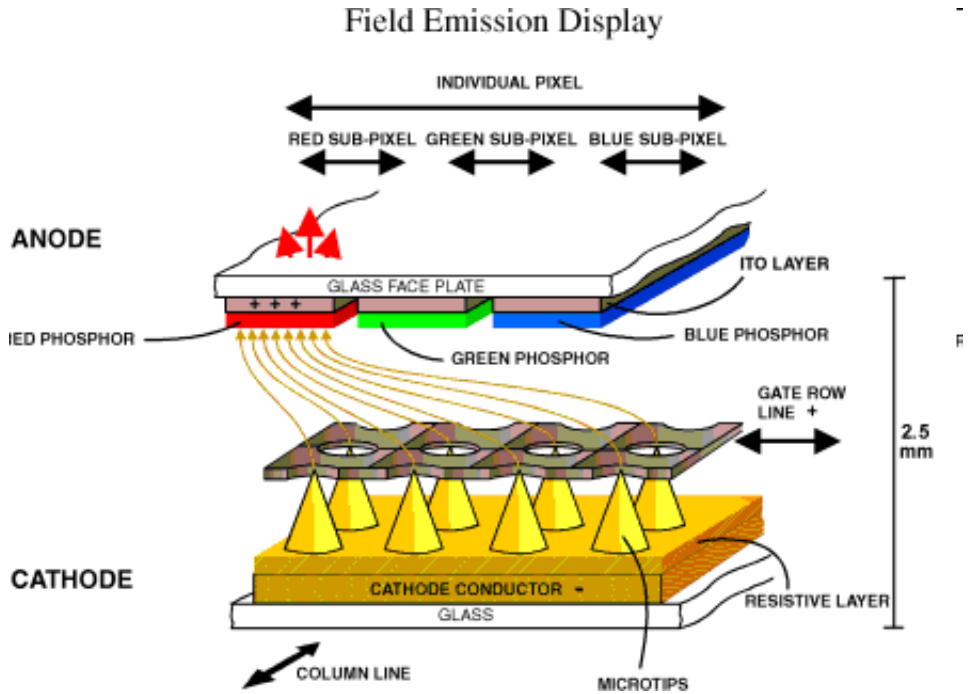


- Passive matrix
- Xe Micro-plasma, 0.5 Bar
- 200 V discharge
- UV light (148/172 nm)
- Phosphors for visible light
- Intensity adjusted by length of pulse
- High voltage
- High consumption
- Phased out

FED



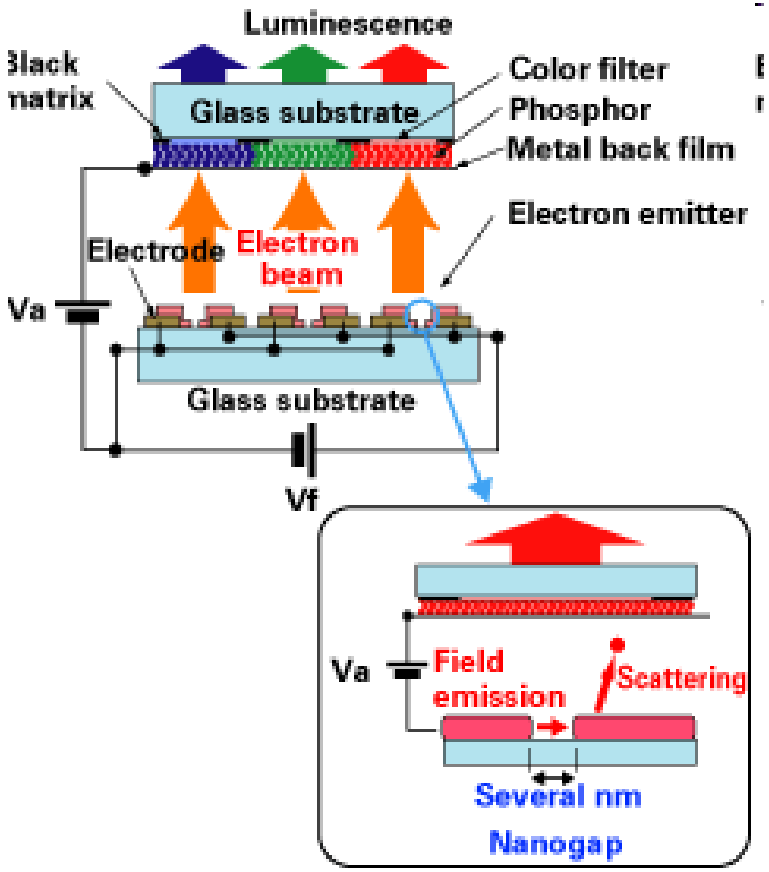
Field Emission Display

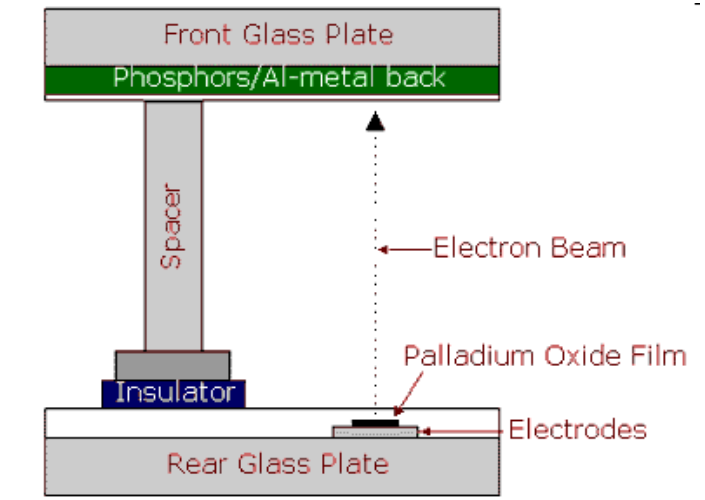


- Works like a CRT with multiple electron guns at each pixel
- Uses modest voltages applied to sharp points to produce strong E fields
- Reliable electrodes proven difficult to produce
- Thin but requires a vacuum
- High consumption

Sony

SED





Simplified Diagram of Canon's Surface-conduction Emission Display

- Similar to FED, different e^- emitter
- Easier fabrication process than FED
- No commercial development due to patent issue
- Development stopped

55" SED HDTV of Toshiba/Canon

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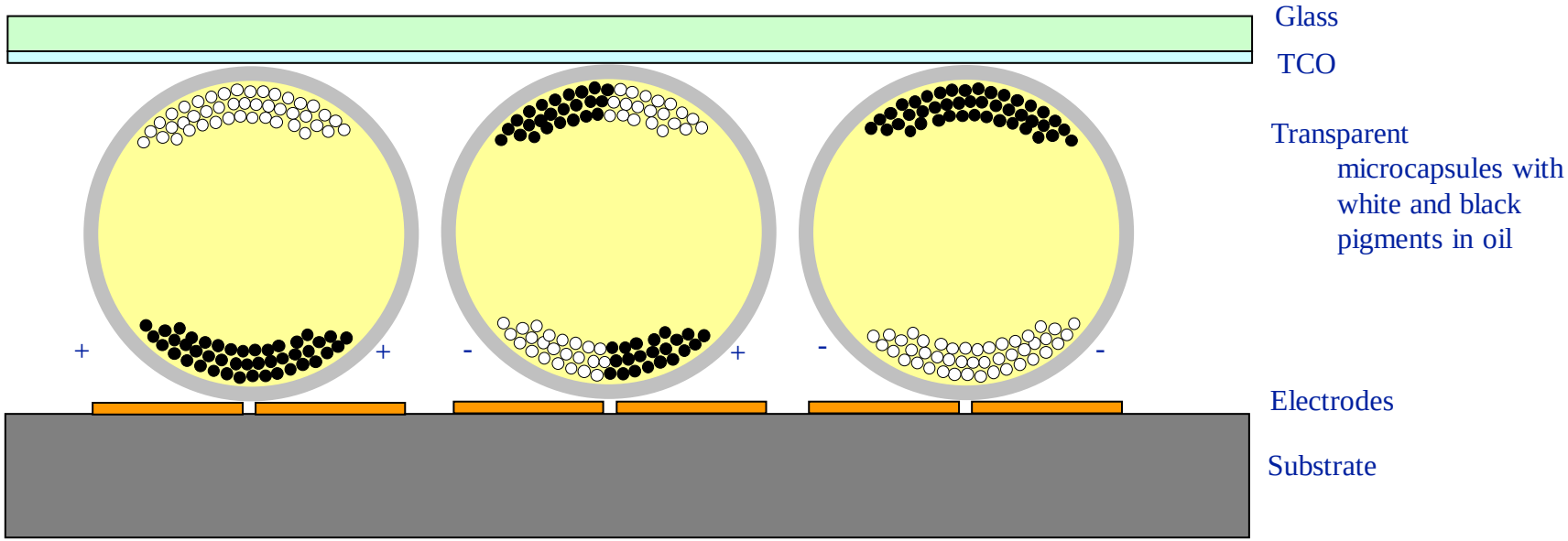
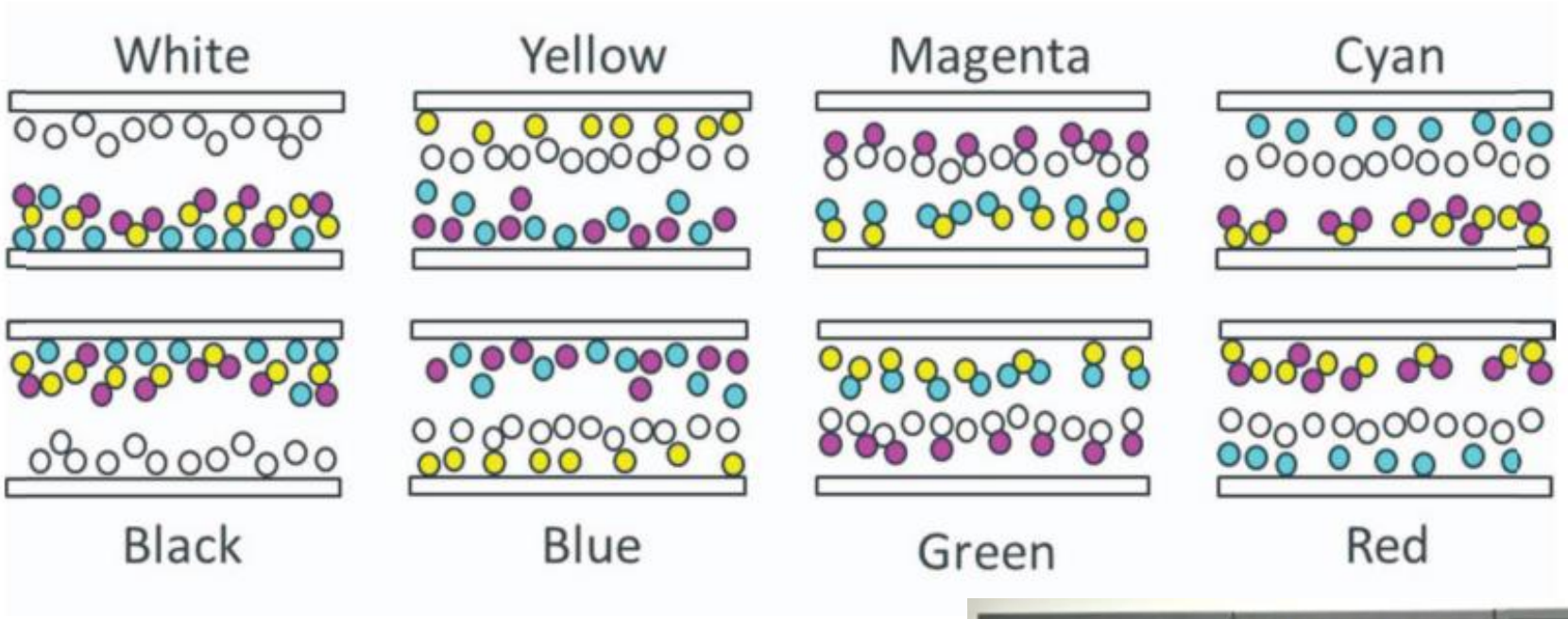
Electrophoretic (e-paper, e-ink)



- Change of pixel color by moving colored beads in transparent or colored liquid
- Color display possible
- Flexible display
- Slow process
- Voltage driven
- Low consumption

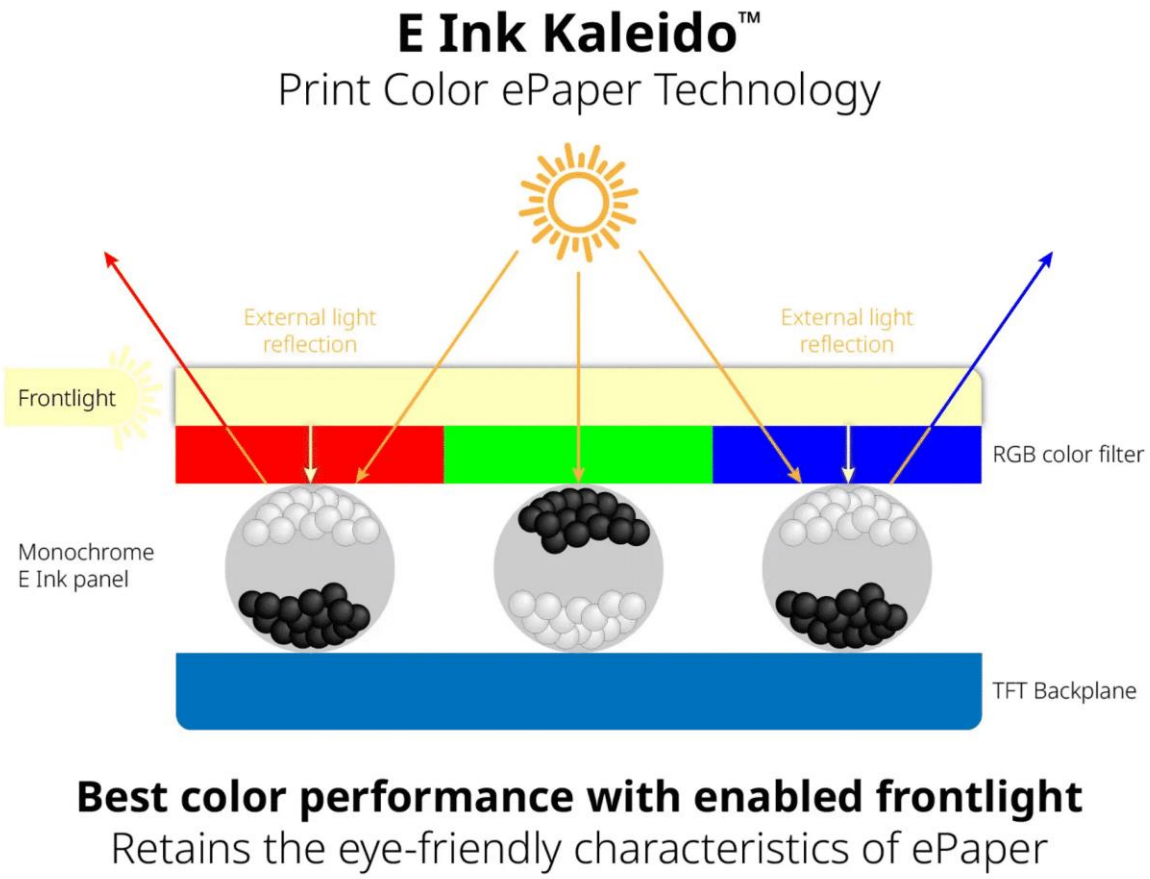
Advanced Color e-Paper (ACeP)

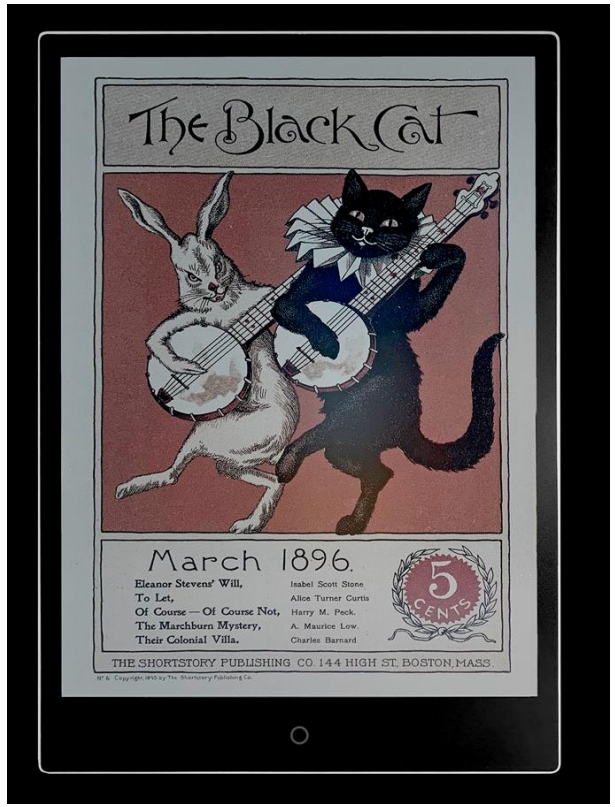


- ACeP plays with electrophoretic mobility of various colored pigments (voltage or current dependance) and polarity dependance

Information Display, review, 2016

Advanced Color e-Paper (ACeP)(2)

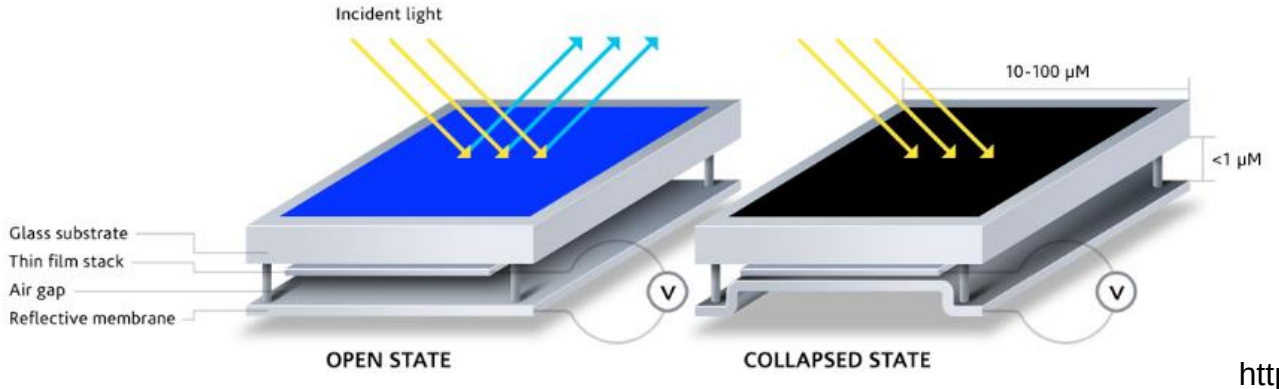


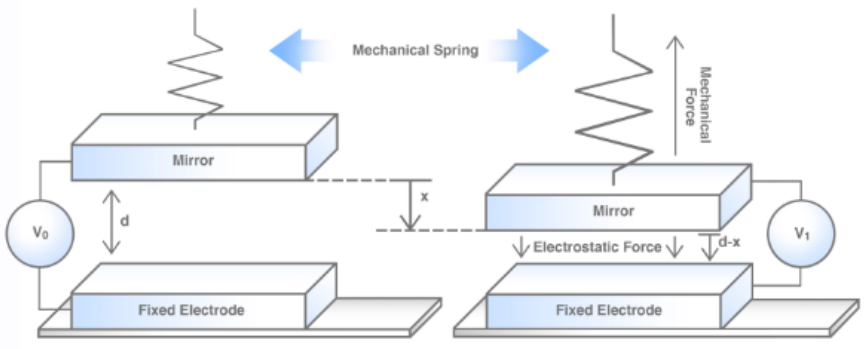


- Colored display possible with colored filters

Interferometric modulator display (IMOD)

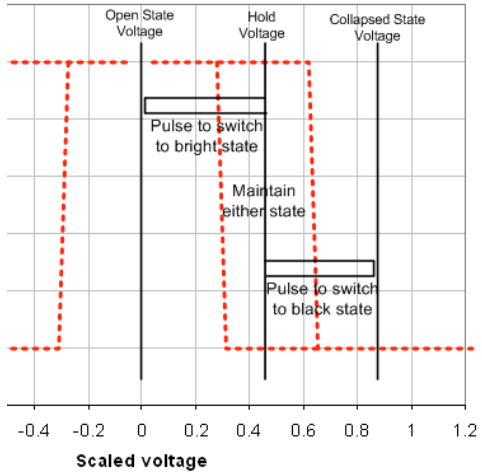
- Based on MEMS driven interferometric cavities

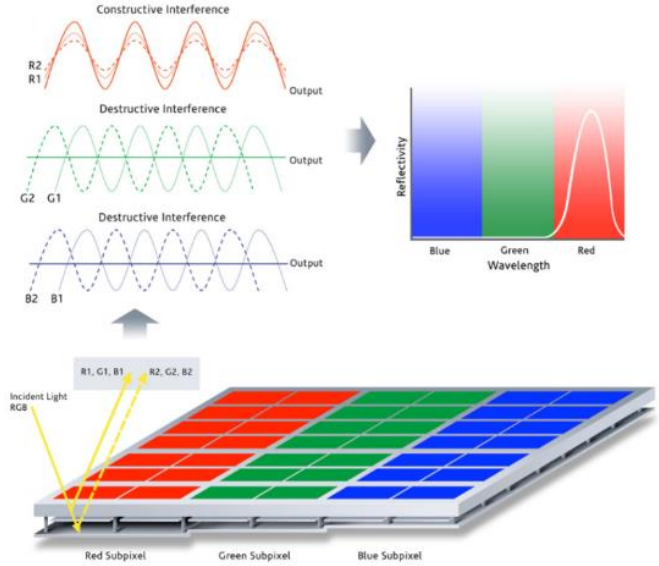




Mirasol® displays, http://www.qualcomm.com/mirasol
http://www.qualcomm.com/media/videos/mirasol-effect-how-it-works

- Quasi bi-stability of cavity state (hysteresis)





- Greyscale generation using either spatial or temporal dithering
- Technology no more actively pursued

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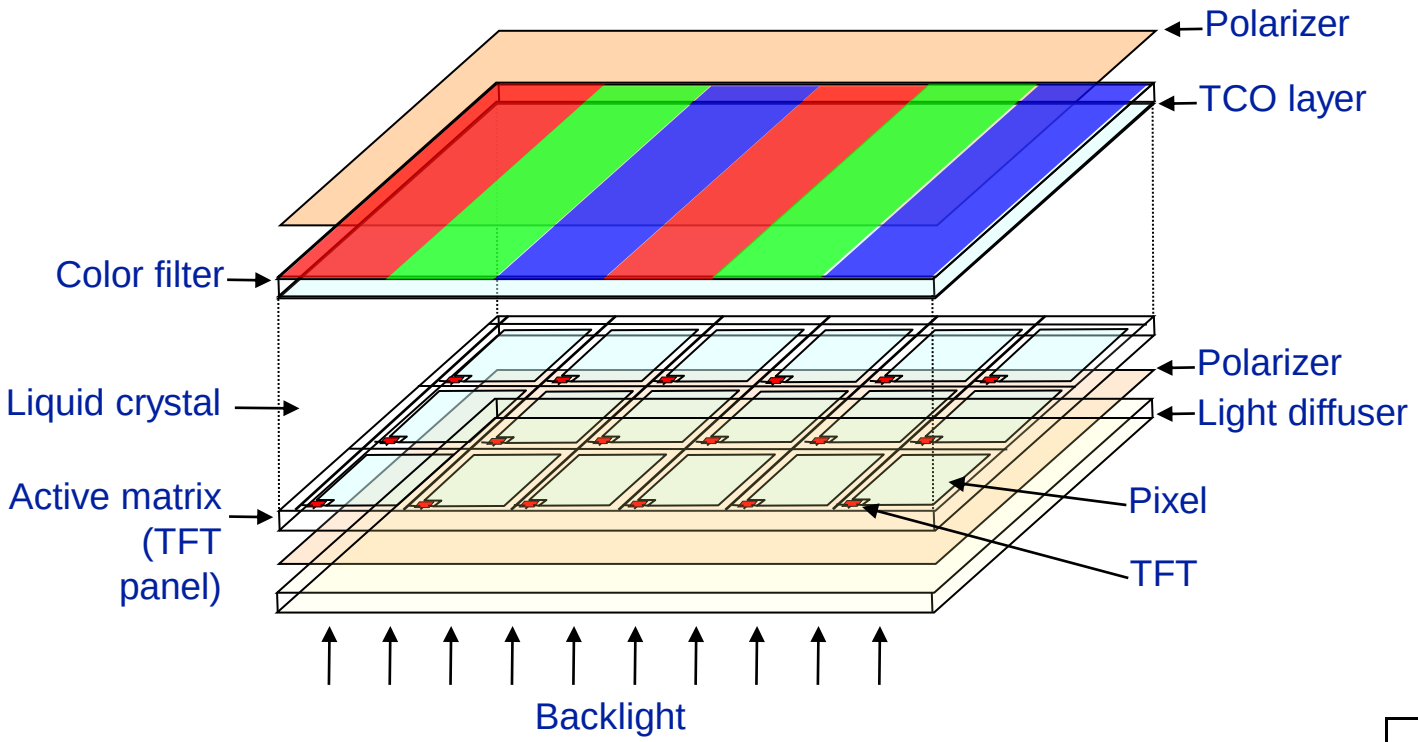
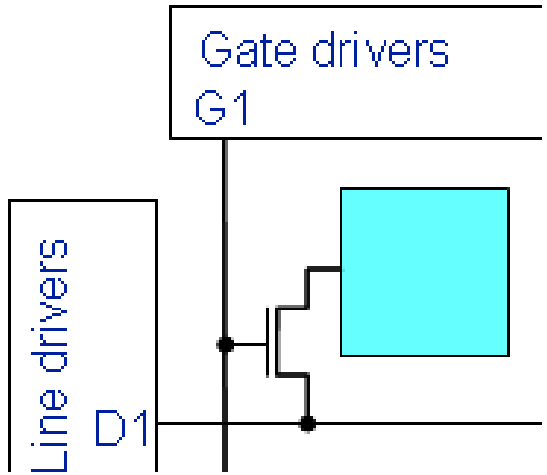
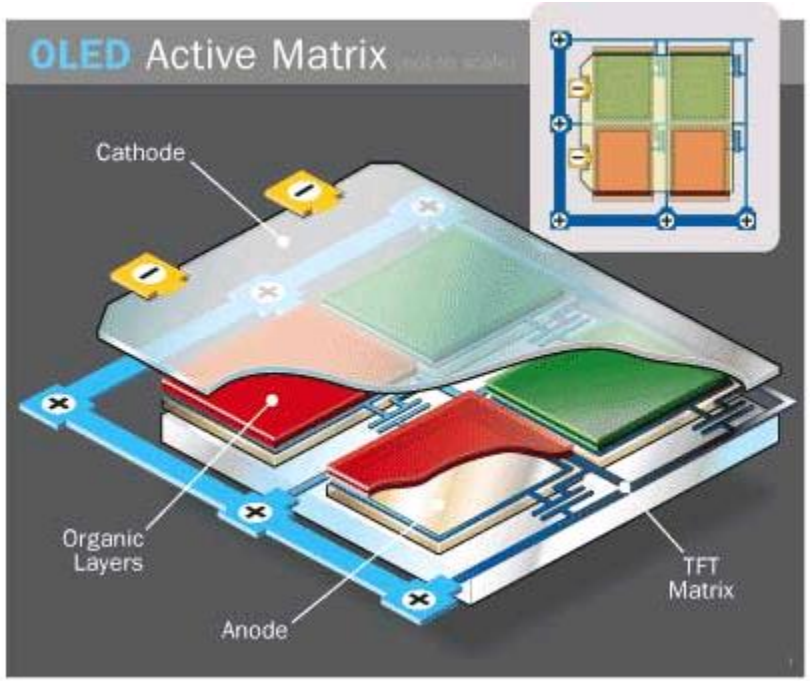
AMLCD

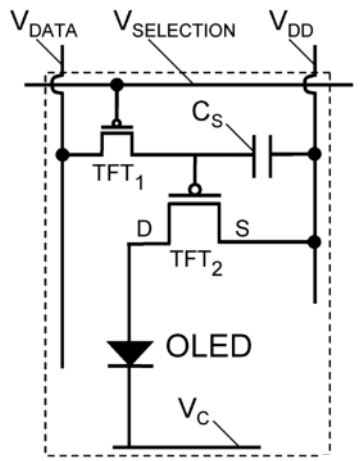


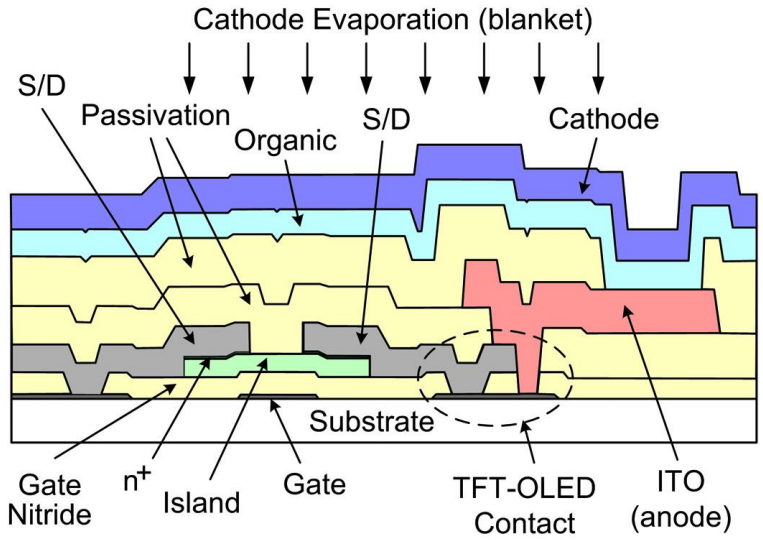


- Voltage controlled LCD cell
- Each column (gate driver) updated in parallel
- Low leakage TFT

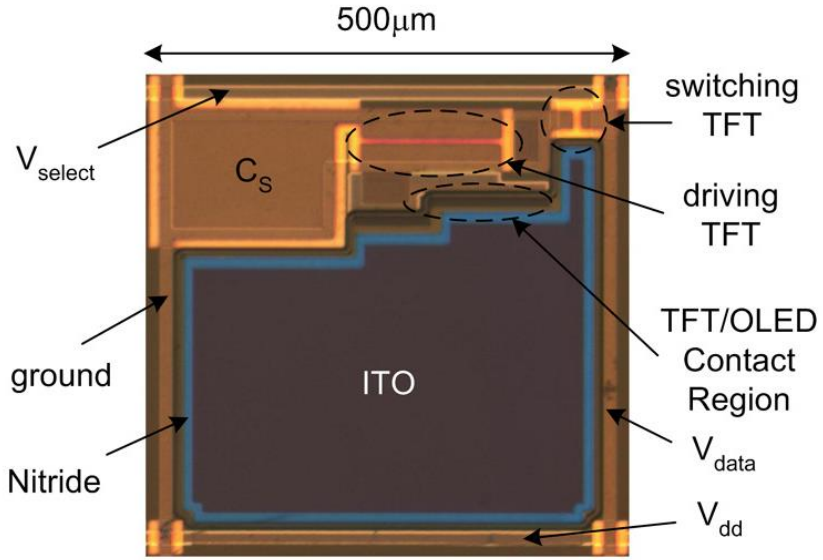
AMOLED







- Voltage or current programming for brightness (and ON/OFF) control
- 2-7 transistor circuit needed
- Circuit to compensate V_{th} drift (≥4 T circuit)
- Each column (gate driver) updated in parallel
- High current TFT (OLDE driver)



AMLCD vs AMOLED

- AMLCD
- Need back light illumination
- Simple (1 T) pixel circuit

- Less sensitive to transistor stabililty

- Voltage driven pixel
- Small area for circuit
- Low mobility material can be used

AMOLED

- « internal » light emission
- Complex pixel circuit (including capacitance)
- Sensitive to transitor characteristic change (stability)
- High current transistor
- Large area needed for circuit
- High mobiliy material desired

TFT requirements for large area electronics

Requirements

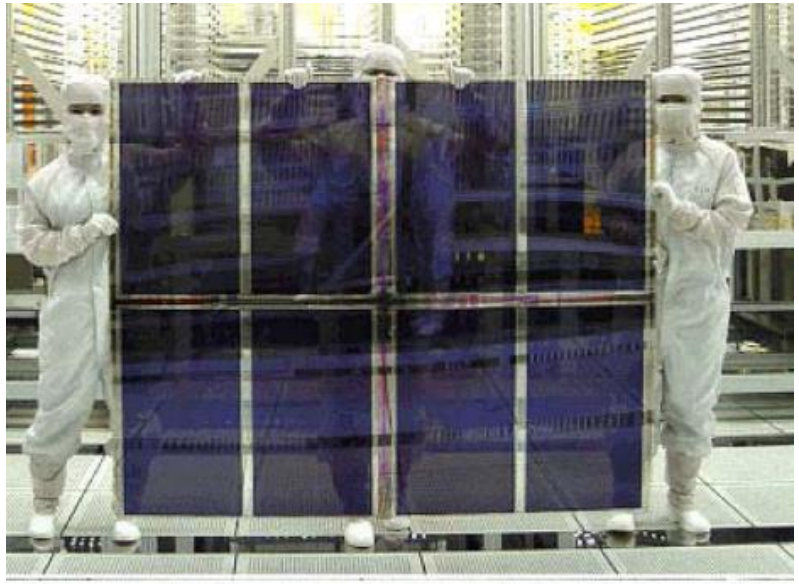
- Low process temperature (substrate dependent):
  ≤ 300 ºC for glass, ≤ 400 ºC for metal foils, ≤ 200 ºC for plastics
- Large area deposition
- TFTs with low leakage current
- High ON/OFF ratio
- Low photosensitivity
- Low voltage operation
- Small device area
- High uniformity
- High stability
- High lifetime

TFT materials

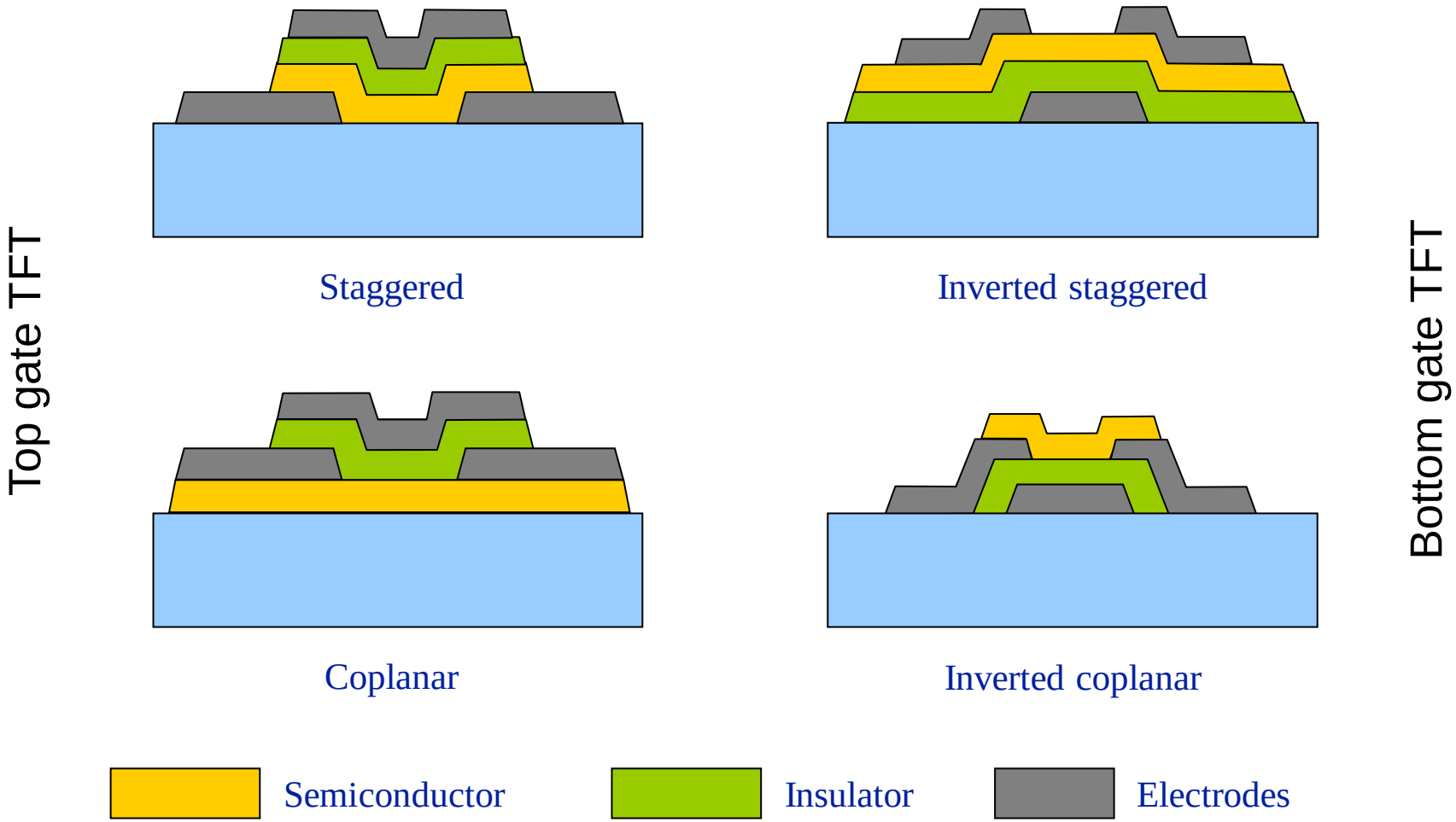
- Early developments
  - CdS
  - CdSe, Te, InSb, Ge
- **Main stream**
  - **a-Si:H**
  - **LTPS (low-temperature poly-Si) (see also specific lecture on LTPS)**
  - **Metal oxides**
- Research or development phase
  - LTPS: process improvements, uniformity
  - Metal oxides (In, Ga, Zn based oxides, …), stability and mobility
  - μc-Si:H, PECVD deposited poly-Si (almost abandoned)
  - Organic materials

a-Si:H TFT features

- Difference between crystalline and amorphous Si materials for TFTs:
  - The free carrier mobilities
    (2 orders of magnitude between a-Si:H et c-Si)
  - the continuous distribution of localized states in the gap of a-Si:H
    → fabrication of bipolar transistors in a-Si:H is not possible
  - High density of traps for free holes
  - Operation frequency limited to ≈100 kHz (due the electron mobility)
- Advantages of a-Si:H
  - low cost
  - low process temperature (250 °C)
  - large area

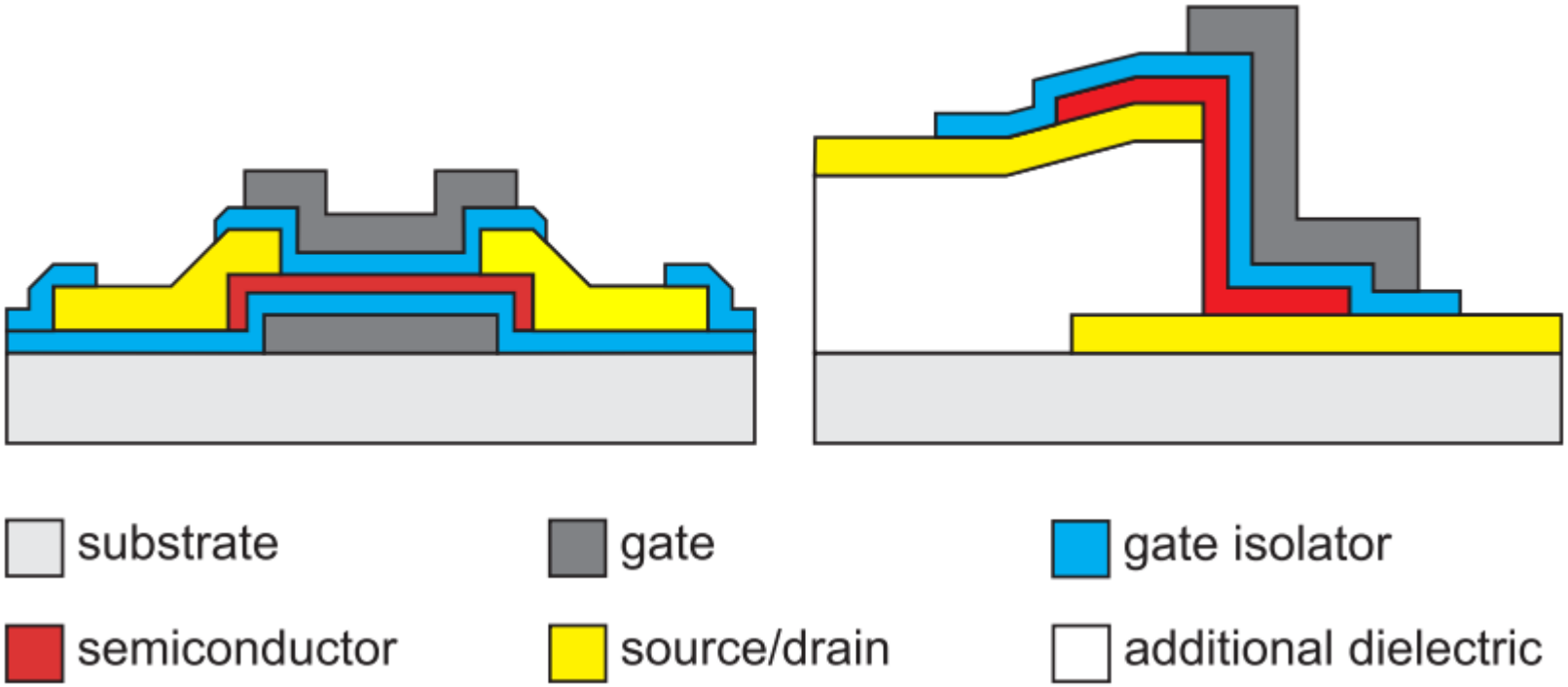


TFT configurations



- Various substrates possible (glass, ceramics, polymers, metal foils,…)

Alternative configuration



Petti et al., Appl. Phys. Rev. 3, 021303 (2016)

Process flow for AMLCD TFT

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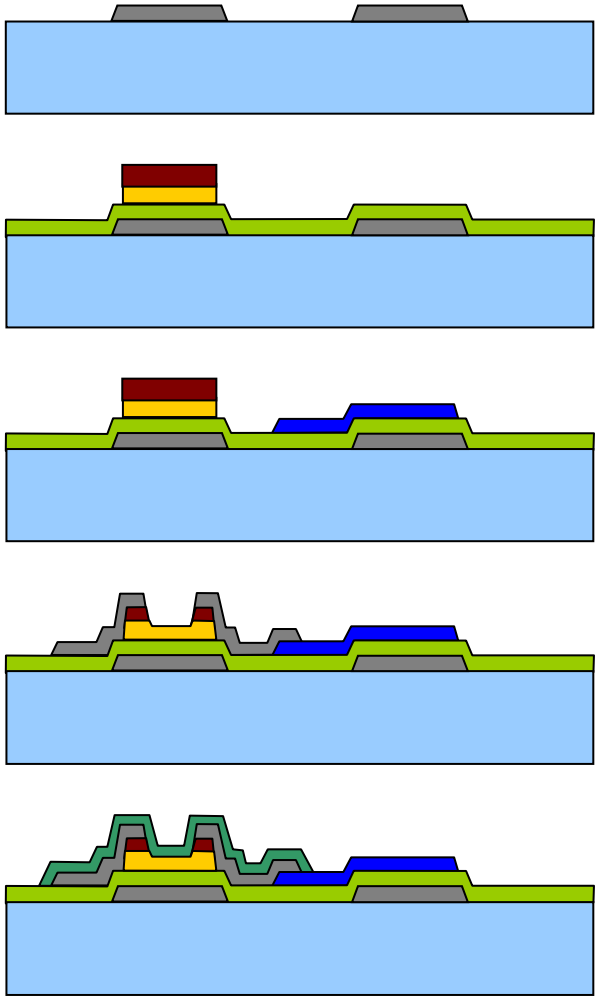


Gate electrode deposition and patterning

Gate dielectric deposition (SiN_x) deposition, a-Si:H stack (intrinsic and n-doped) deposition and patterning

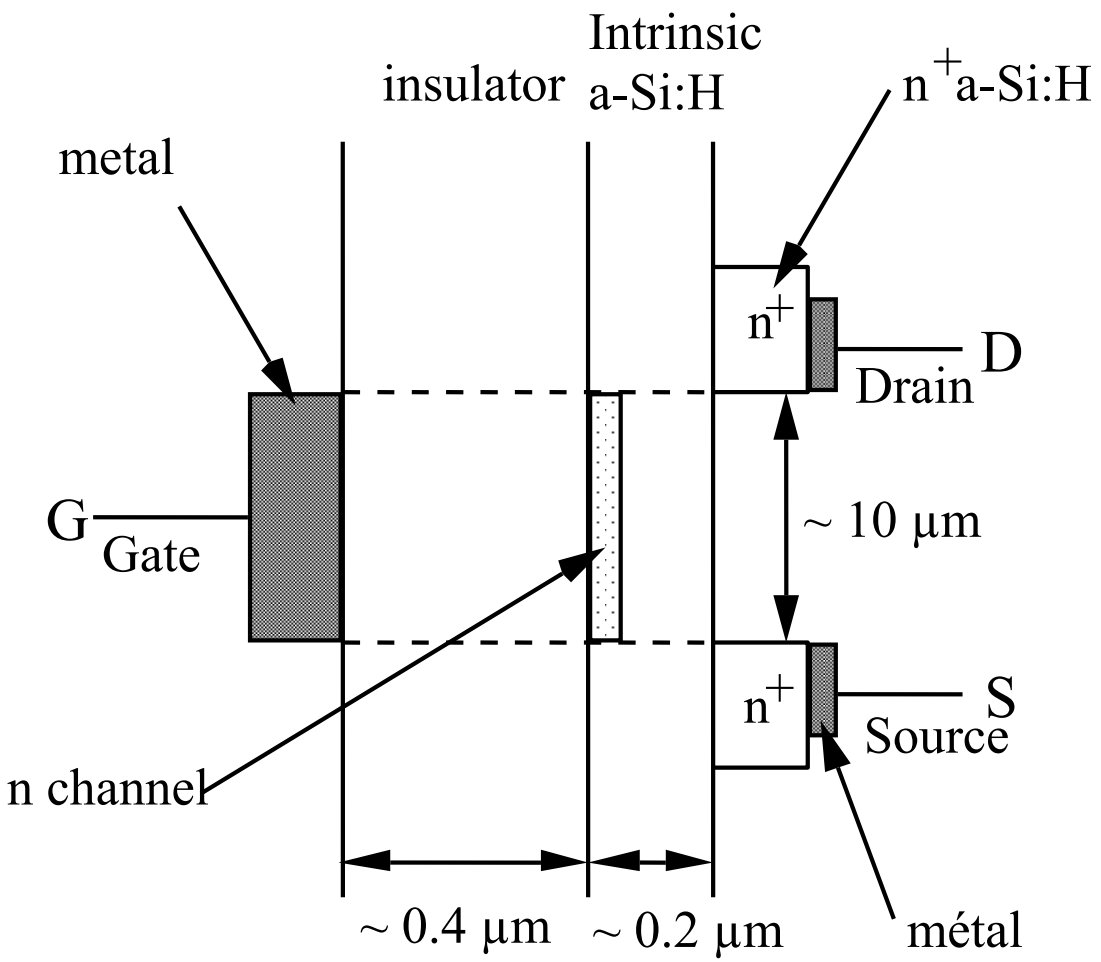
ITO (pixel contact) deposition and patterning

Source/drain metal deposition and patterning

Passivation layer deposition and patterning.

Layer	*Thickness [nm]*
Gate metal	130
a-SiN_x gate dielectric	250
a-Si:H	50
a-SiN_x passivation layer	250
n^+ μc-Si:H contact layer	30
Metal contact layer	500

Schematic of a-Si:H TFT



- very low conductivity of the intrinsic layer (high gap of a-Si:H)
- n-type channel
- structure of the TFT (gate/insulator/channel) is similar to the one of a capacitor
- capacitive behavior between the gate and the other transistor electrodes (drain and source)
- This behavior depends on the gate potential V_G

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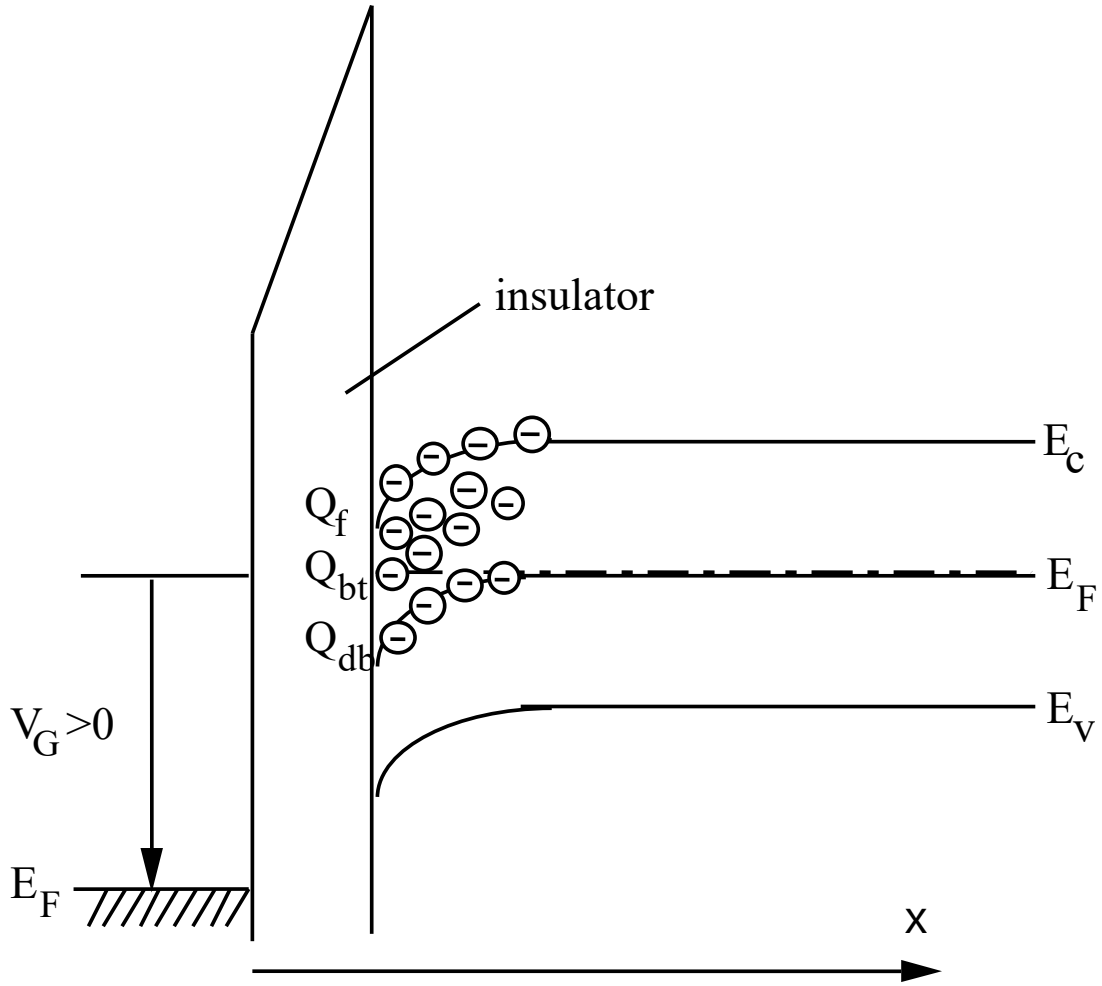
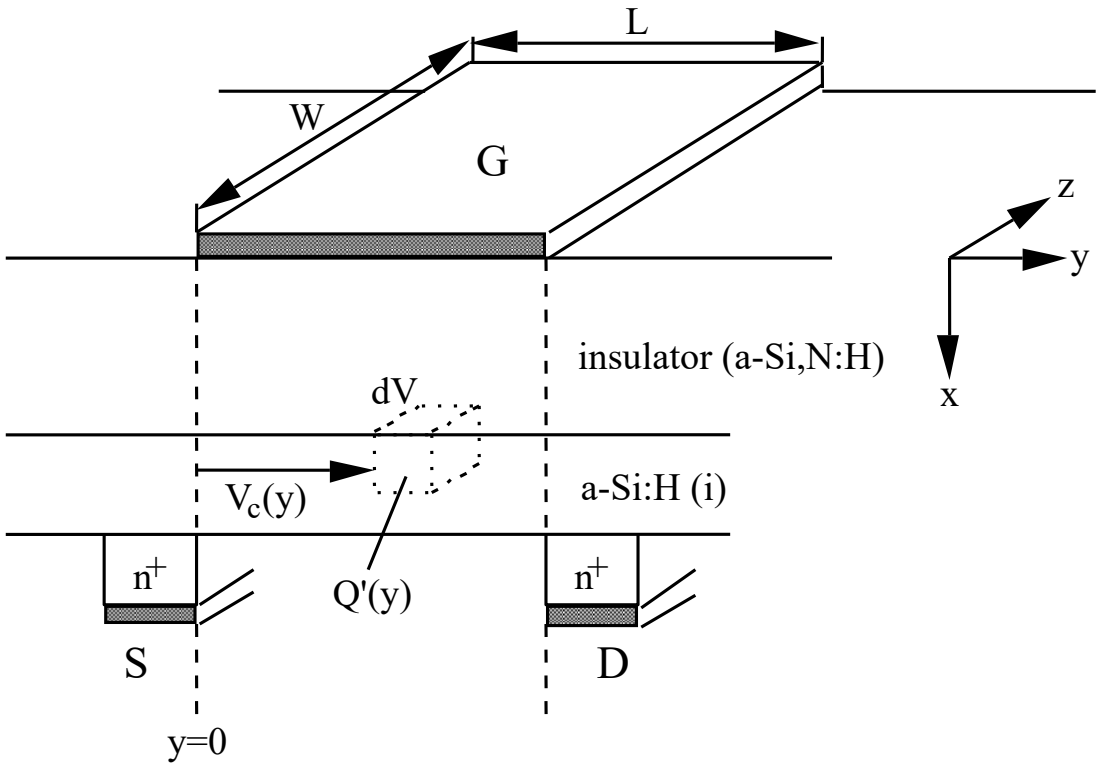
Operation of a-Si:H TFT



- For $V_G > 0$
- When $V_G > V_T$ (threshold voltage)
  → formation of a **n-type conduction channel** ([change from i → n], called inversion channel in the case of c-Si transistors [change from p → n], in the semiconductor).
- $Q_{tot} = C \cdot V$
  with $Q_{tot} = Q_f + Q_{bt} + Q_{db}$
- where C is the total capacitance of the insulator defined by the gate and channel.

Calculation of TFT characteristics



- charge per unit area (at a point y of the conduction channel)

$$V_G - V_T(y) = \frac{Q'_{tot}(y)}{C'_{nitride}}$$

- Total charge Q'_{tot}

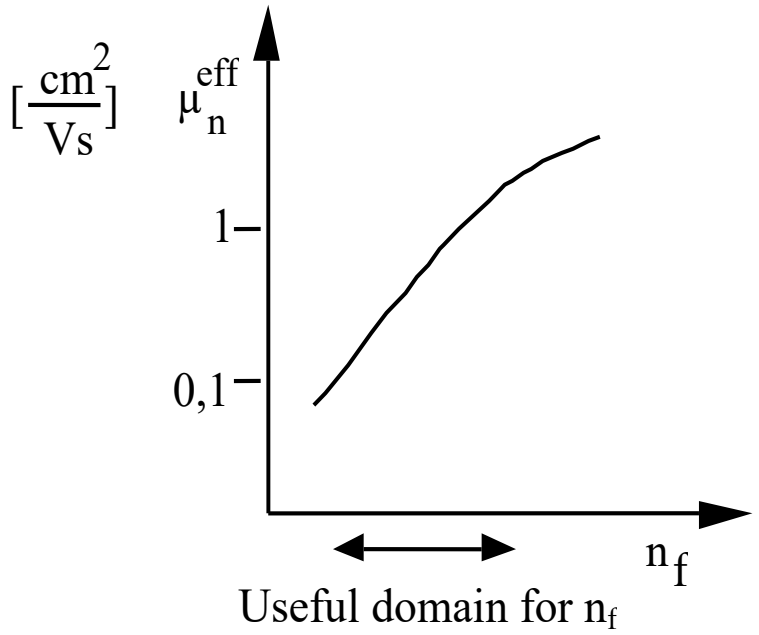
$$Q'_{tot}(y) = q \int_{channel} n_{tot}(x,y)dx =$$

$$= q \int_{channel} \left(n_f(x,y) + n_{bt}(x,y) + n_{db}(x,y)\right)dx$$

- Drain-source current (no diffusion)

$$I_{DS} = \int_{channel} q\mu_n^0 n_f(x,y)F_y(y)dxdy$$

Effective mobility



μ_n^o - 10...20 $\frac{cm^2}{Vs}$

μ_n^{eff} - 0.1...2 $\frac{cm^2}{Vs}$

- Effective mobility of the total carrier density (to relate I_{DS} with the total charge):

$$\mu_n^0 n_f(x,y) = \mu_n^{eff}(x,y) n_{tot}(x,y)$$

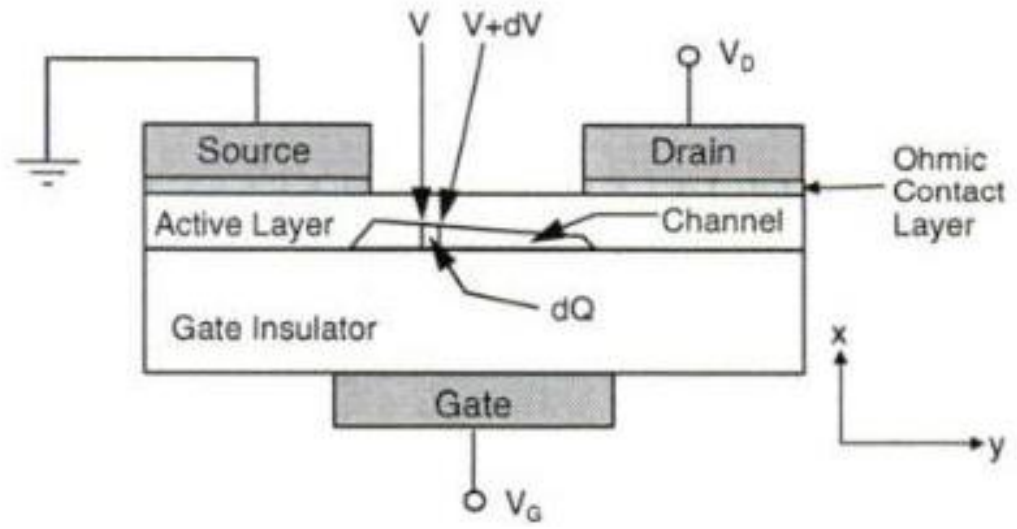
- Drain-source current

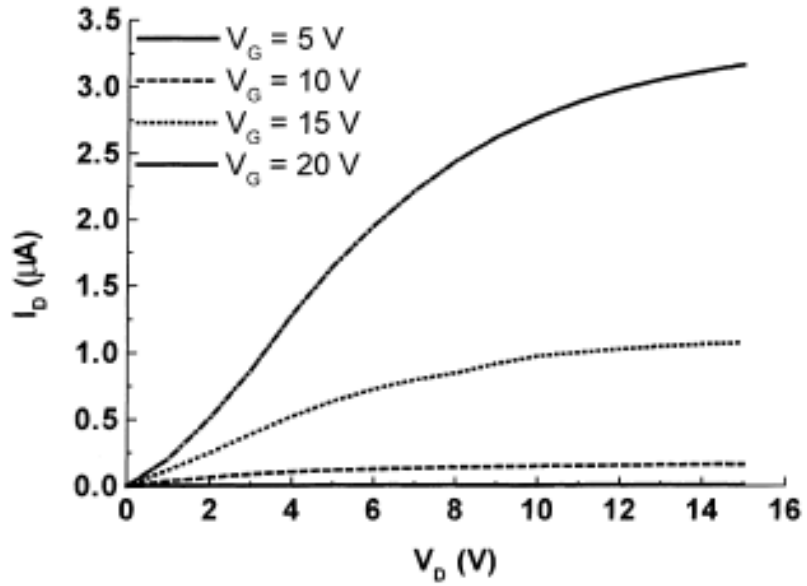
$$I_{DS} \approx \int_{channell} q\mu_n^{eff}(x,y) n_{tot}(x,y) F_y(y) dxdy$$

- Simplified model

$$I_{DS} \approx \int_{channel} q\mu_n^{FET} n_{tot}(x,y) F_y(y) dxdy$$

TFT regimes





- Off-state regime

  $V_G < V_{Th}$

- Linear regime for

  $V_{DS} << V_G$

  – Charge per unit area allong the channel assumed constant

- Saturation regime for

  $V_{DS} \approx V_G - V_{Th}$

  – Pinching of channel

N. Wyrsch

Transconductance (linear regime)

- Simplified model (global value μ^{FET})

$$I_{DS} \approx \int_{channel} q\mu_n^{FET} n_{tot}(x,y) F_y(y) dxdy$$

$$I_{DS} \approx \mu_n^{FET} F_y(y) \int_{channel} q n_{tot}(x,y) dx \int_0^W dy$$

$$I_{DS} \approx W\mu_n^{FET} F_y(y) Q'_{tot}(y)$$

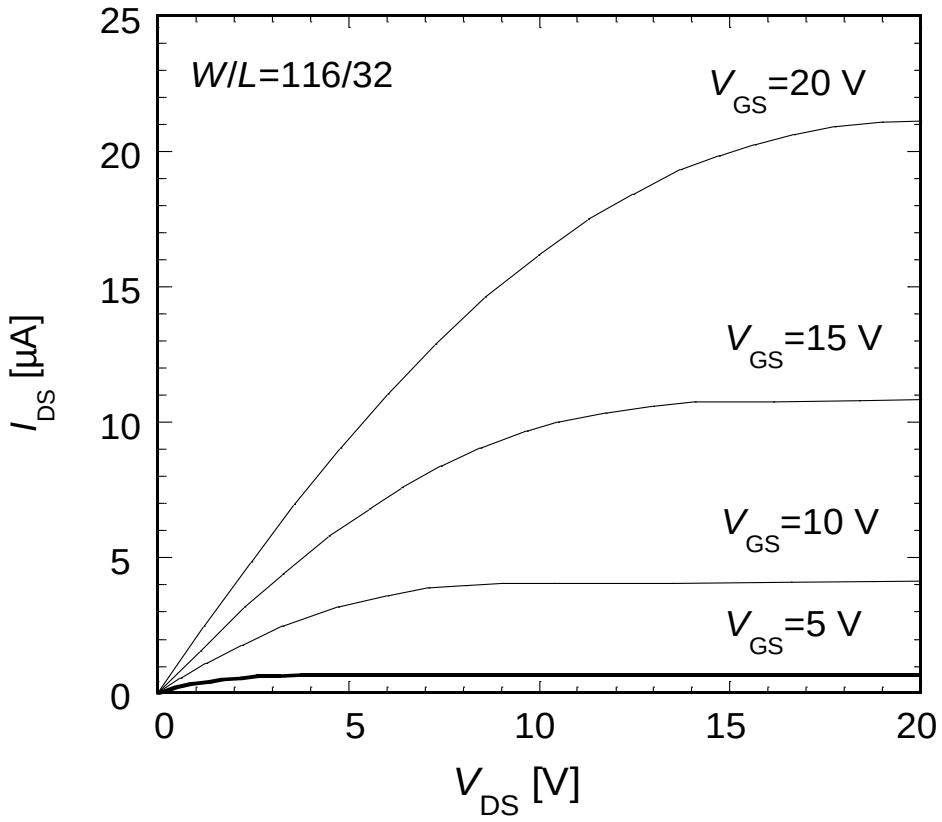
- Field along the channel: $F_y(y) \approx C^{ste} \approx \frac{V_{DS}}{L}$

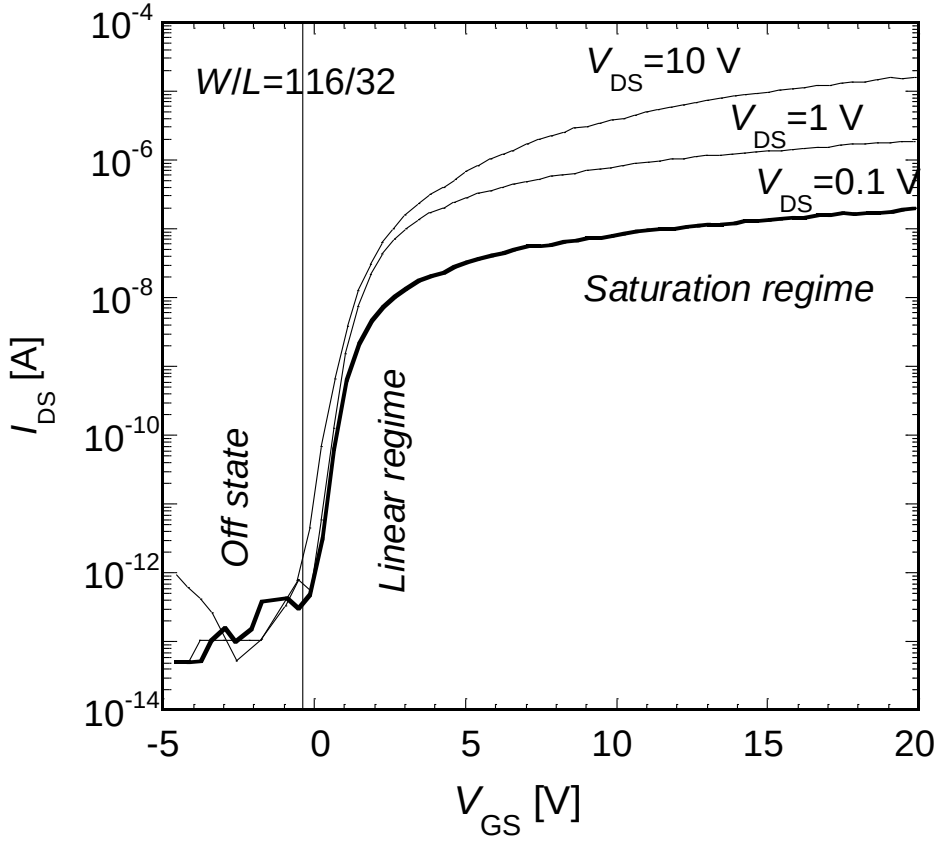
$$I_{DS} \approx \mu_n^{FET} \frac{W}{L} C'_{nitride} (V_G - V_{T,mean}) V_{DS}$$

- Transconductance (allows the determination of μ^{FET})

$$\frac{\partial I_{DS}}{\partial V_G} \approx \mu_n^{FET} \frac{W}{L} C'_{nitride} V_{DS}$$

Operation of a-Si:H TFTs

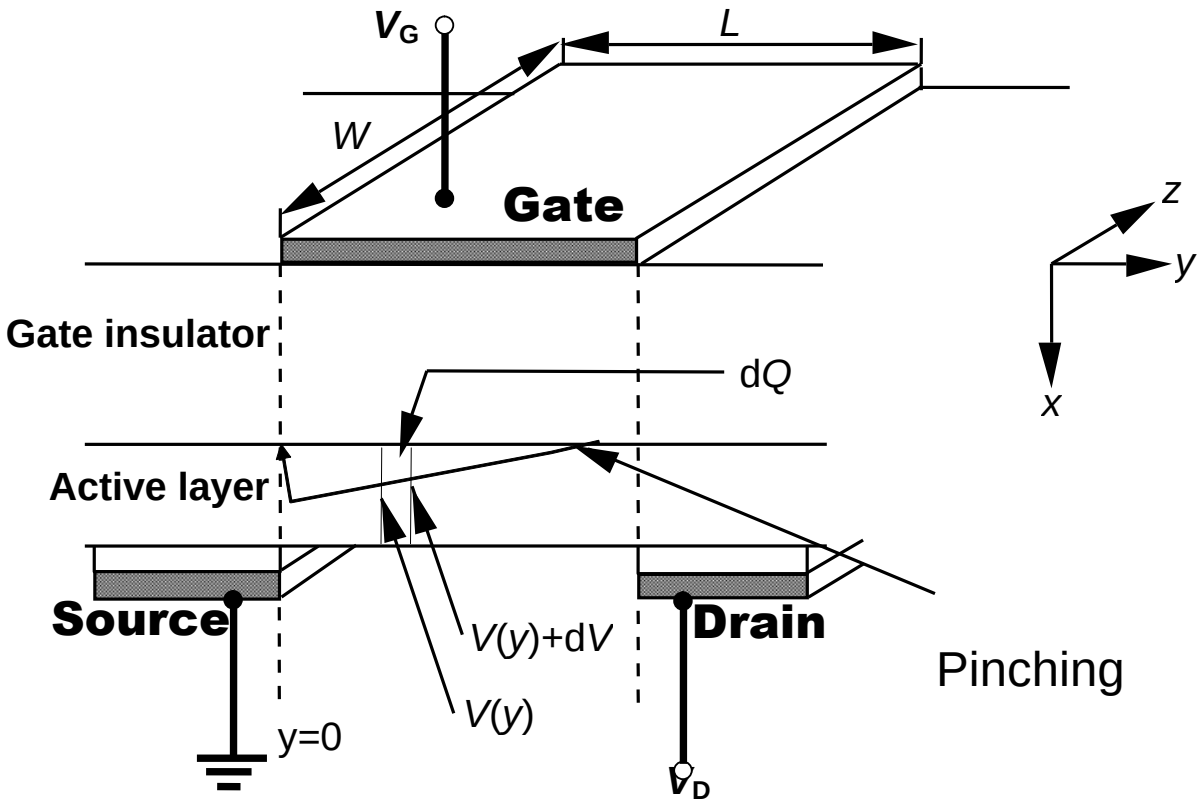




Linear regime

$$I_{DS} \approx \mu_n^{FET} \frac{W}{L} C'_{SiN_x} \left(V_G - V_{TH}\right) V_{DS}$$

Saturation regime



Pinching

- For $V_{DS} \geq V_G - V_{Th}$ pinching of channel
- Variation of potential allong the channel has to be taken into account

$$I_{DS} \approx \mu_n^{FET} \frac{W}{2L} C'_{nitride} (V_G - V_{th}^{mean})^2$$

Important parameters

- μ_n^{FET}
  - Typical value for a-Si:H: 0.1 – 2 cm^2/Vs
  - Depends on density of states
- V_{TH}
  - Typical value for a-Si:H 2.5 – 50 V
  - Depends on density of states
- I_{ON}/I_{OFF}
  - Typical value for a-Si:H: 10^6
  - Depends on W/L
- Gate Voltage Swing
  - Typical value for a-Si:H: 0.5 V/dec
  - Depends on W/L

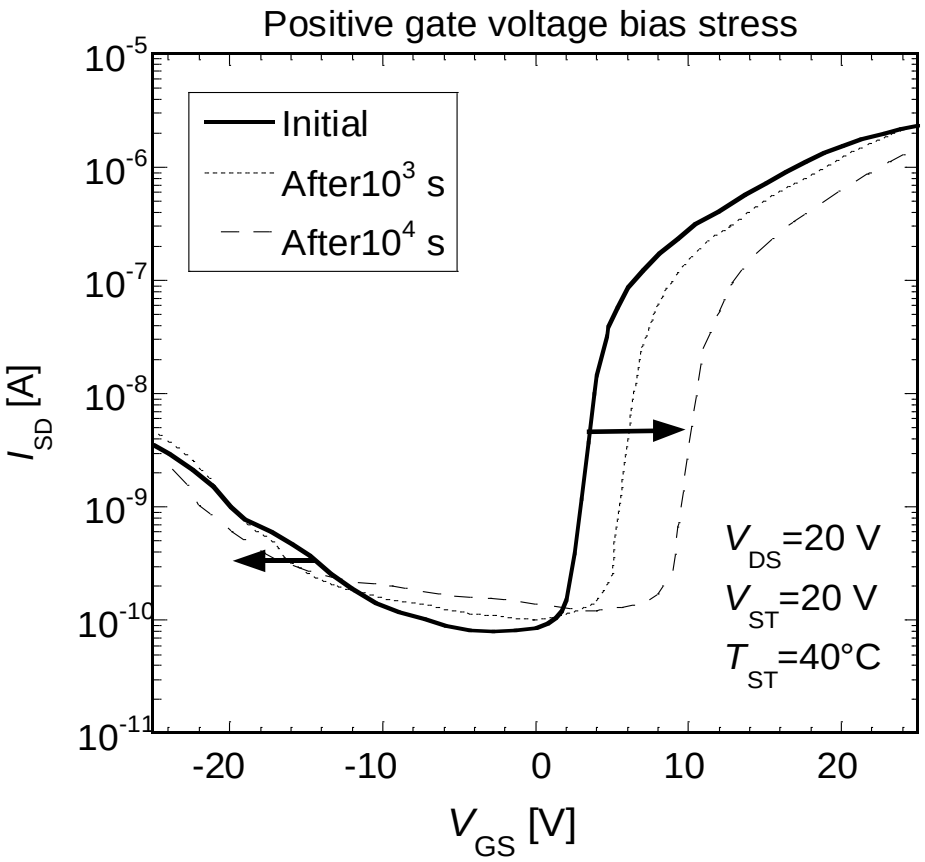
$$I_{DS} \approx \mu_n^{FET} \frac{W}{L} C'_{SiN_x} \left(V_G - V_{TH}\right) V_{DS}$$

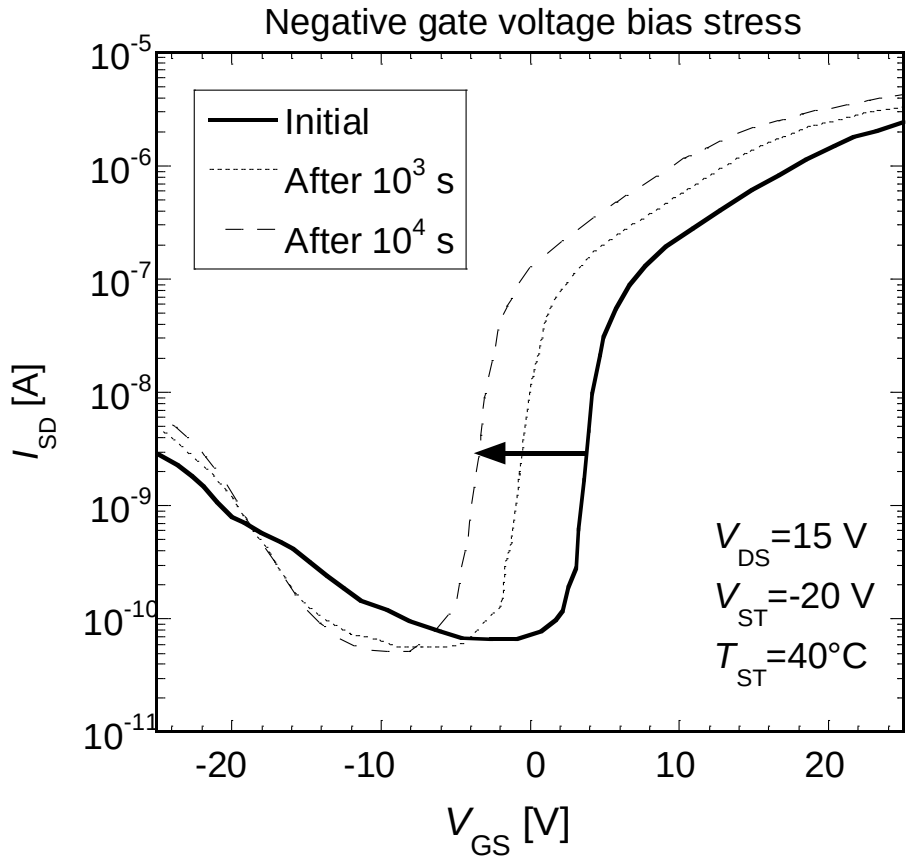
$$\mu_n^{FET}\left[cm^2/Vs\right] = \frac{\partial I_{DS}}{\partial V_G} \frac{L}{W \cdot C'_{SiN_x} V_{DS}}$$

Linear regime

$$S\left[V/Decade\right] = \frac{dV_G}{d\left(\log I_D\right)}$$

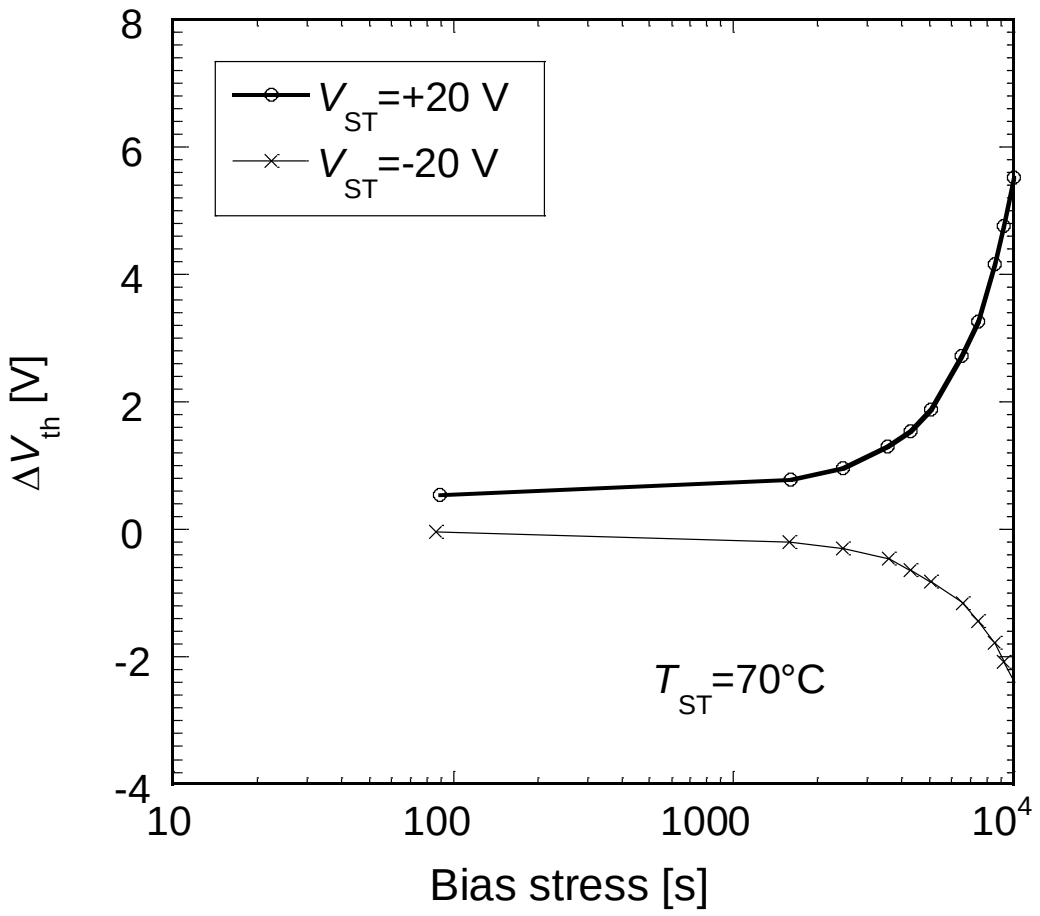
a-Si:H TFT instabilities





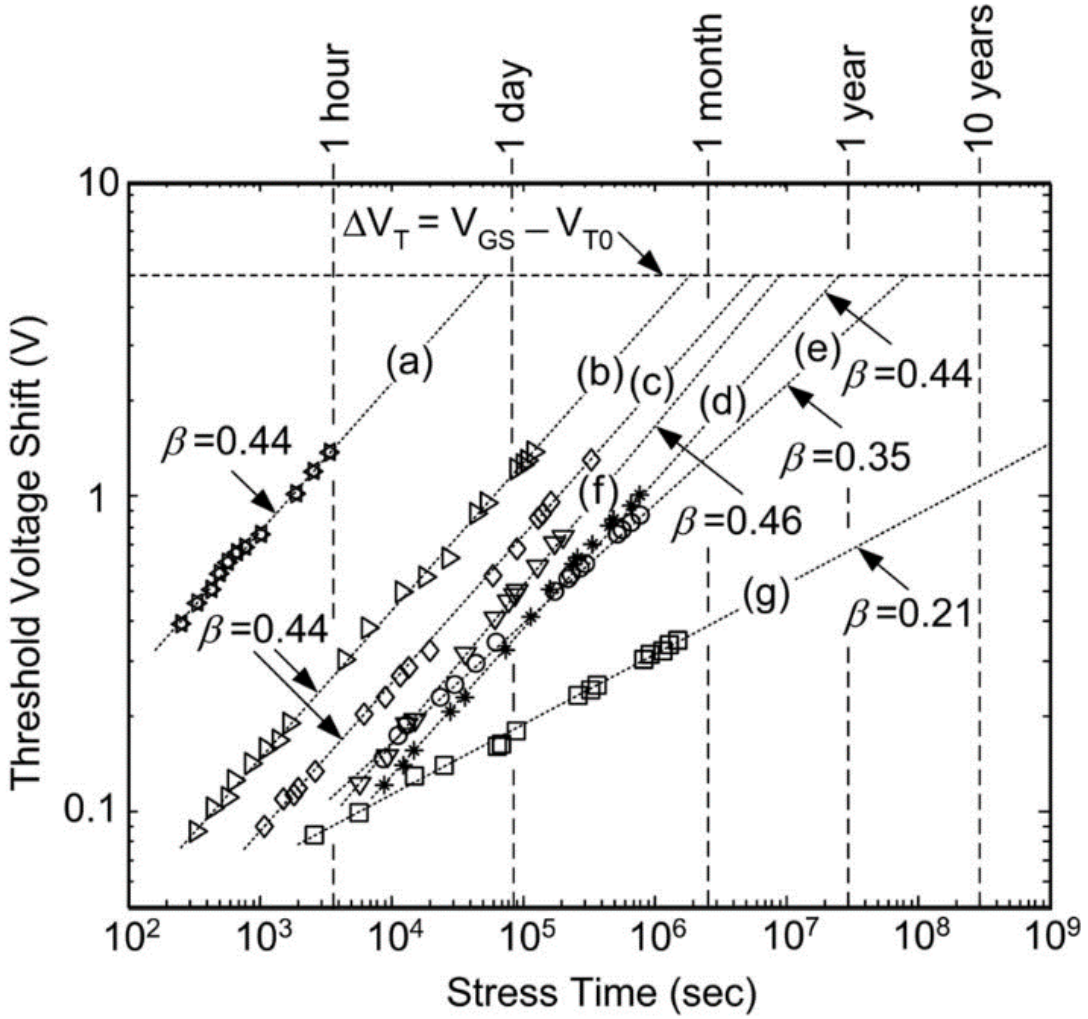
Application of a gate bias during extended time (bias stress)

TFT instabilities



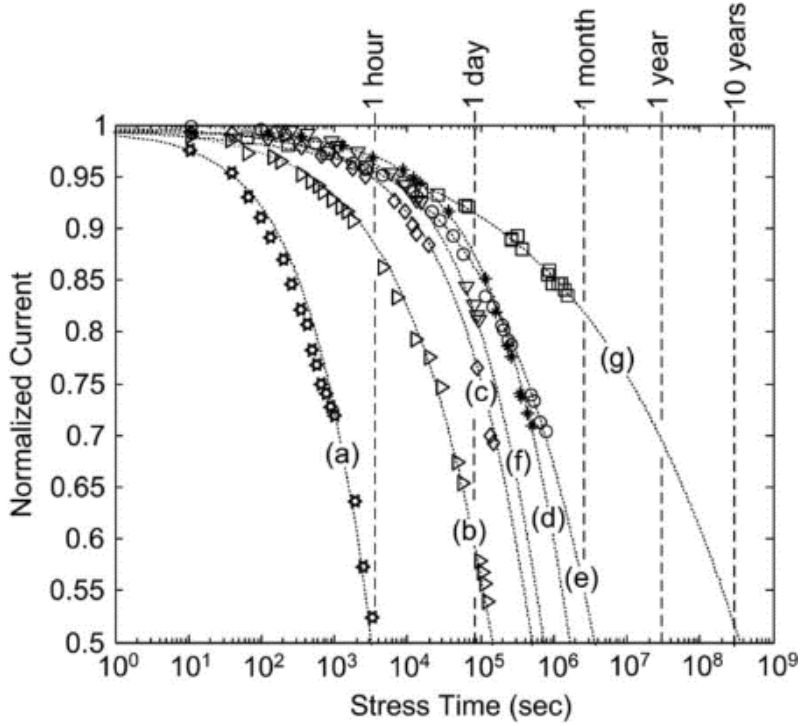
- a-Si:H TFTs usually exhibit instabilities related to shifts in V_T upon bias stress.
- Instabilities are due to
  - charging of the defects in the insulator (usually a-SiN_x:H) (which affects the polarization of the channel)
  - creation of defects in the a-Si:H layer (channel, effect similar to the Staebler-Wronski effect)
- Effect can be reduced by improving the silicon nitride quality (deposition at higher temperature, ≈350°C) and the a-Si:H/a-SiNx:H interface (plasma treatments).

Stability

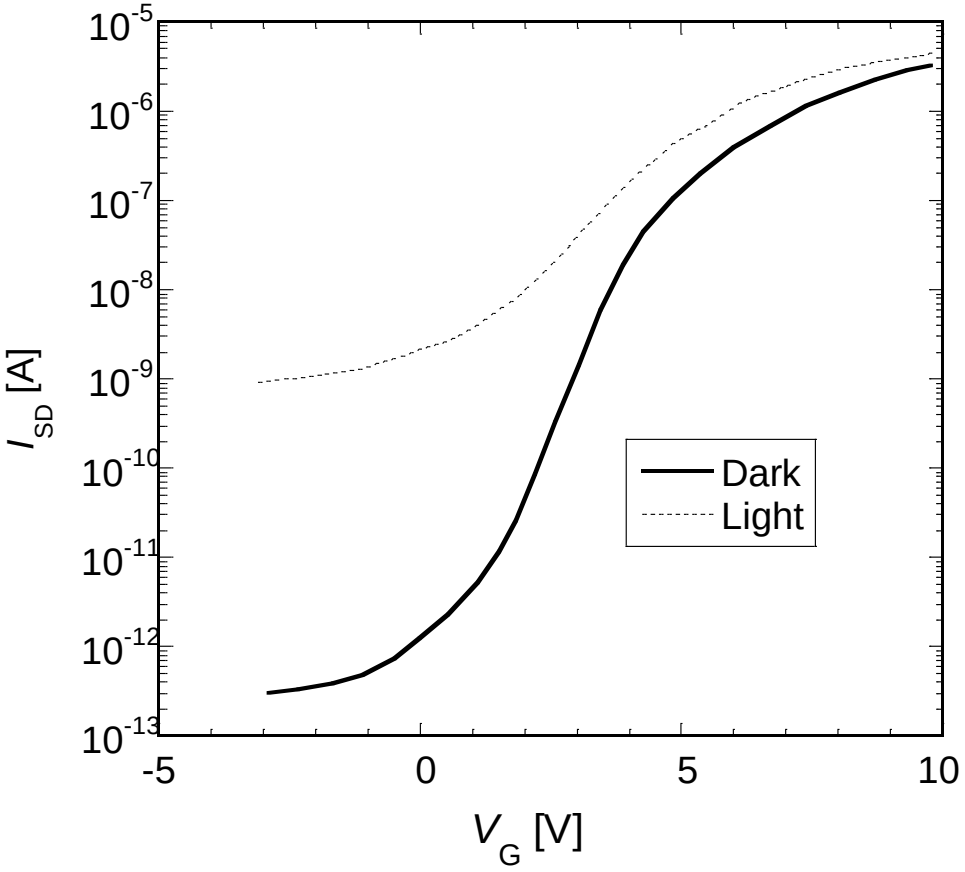


B. Hekmatshoar et al. APL 93, 2008

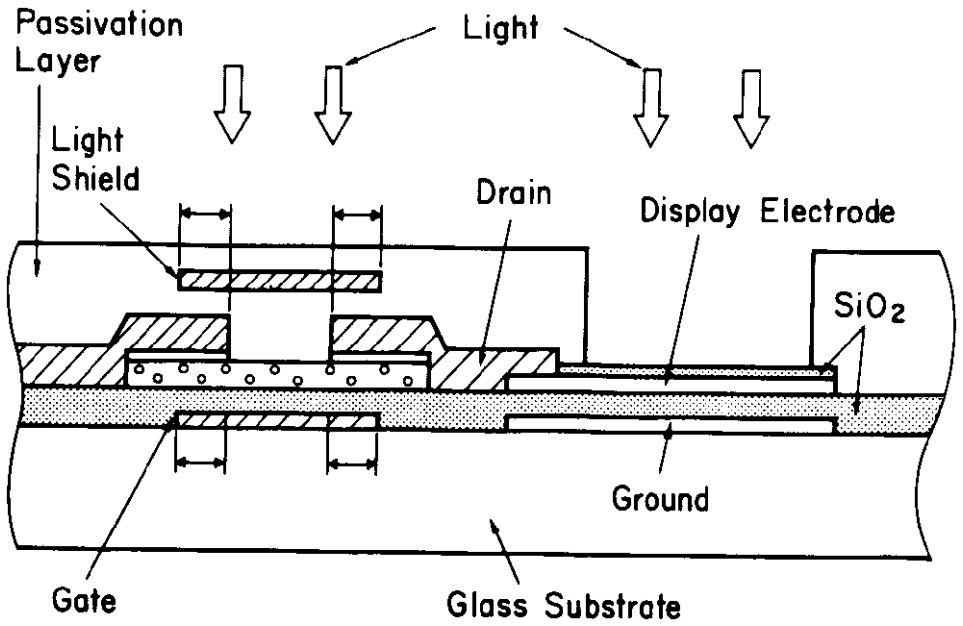
- Analysed in terms of V_{th} shift
- $\Delta V_{th} \propto t^{\beta}$ with β constant at a given stress field
- β depends on the processing and materials
- Deposition at higher temperature with H dilution improve stability (similar to a-Si:H solar cells)



Photosensibility



- Photosensibility of a-Si:H TFTs. Can be reduced by using inverted structure or light shield



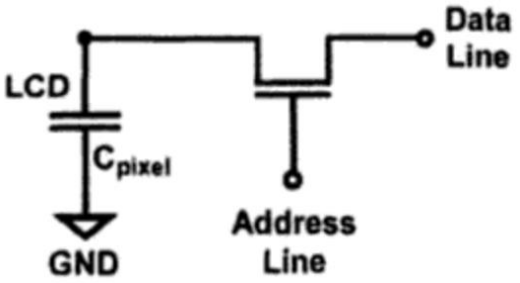
TFT performance

TFT performance	Dominant factor
On-current	W/L · Drift mobility · Interface states (a-Si:H/SiN_x) · Ohmic contact · Gap state density · Back interface states
Off-current	W/L · Fermi level (a-Si:H) · Interface states (a-Si:H/SiN_x) · Back surface charge · n^+ contact (n^+ a-Si:H) · Band gap
Field-effect mobility	Width of band tails (disorder) · Interface states (a-Si:H/SiN_x)
Gate voltage swing	Gap states (defect states) · Interface states (a-Si:H/SiN_x)

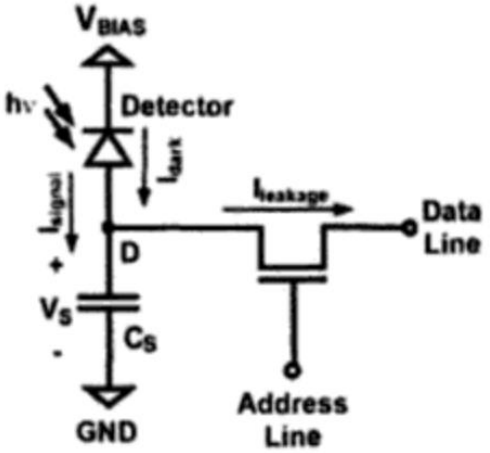
Factors influencing a-Si:H TFT performance

TFT circuits and requirements

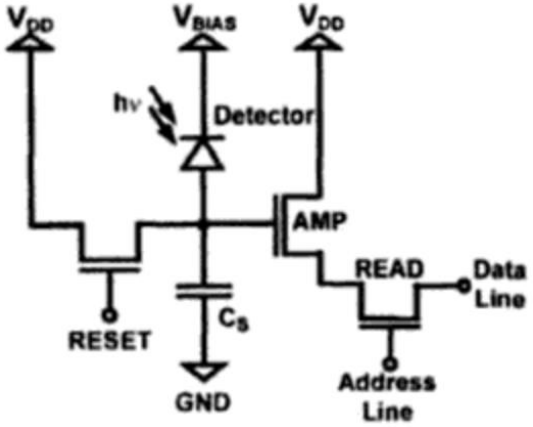
LCD pixel



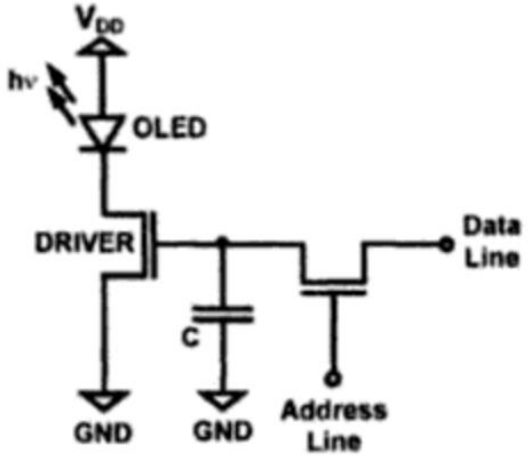
Passive pixel sensor



Active pixel sensor



AMOLED pixel



TFT parameter	AMLCD	AMOLED	PPS imager	APS image
V_T	Should be as low as possible			
ΔV_T	Not as critical as in imaging apllications since LCD is non-conducting	Ideally 0	small	small
S		Low	low	low
I_{ON}		High	Not critical	Can be critical
ON/OFF ratio		Large	large	large
$I_{leakage}$		Can be critical	Ideally 0	Ideally 0

A. Nathan, in Thin Film Transistor Technologies VI (2002)

TFT Requirements for AMLCD

On current:

$$I_{on} \geq \frac{6C_{pixel}V_{on}N_{row}}{T_{frame}}$$

Off current:

$$I_{off} \leq \frac{C_{pixel}\Delta V_{on}}{N_{gray}MT_{frame}}$$

On-to-*Off* ratio:

$$\frac{I_{on}}{I_{off}} \geq \frac{6MN_{row}V_{on}N_{gray}}{\Delta V_{on}}$$

C_{pixel}	Pixel capacitance
M	Safety margin coefficient
N_{gray}	Number of gray levels
N_{row}	Number of rows
T_{frame}	Frame period
V_{on}	Gate voltage swing
ΔV_{on}	Required switching voltage

M. Shur, M. Jacunski, H. Slade, M. Hack, "Analytical Models for Amorphous and Polysilicon Thin Film Transistors for High Definition Display Technology," *J. of the Society for Information Display*, vol. 3, no. 4, p. 223, 1995

TFT : materials and performance

	Poly-Si, LTPS	µc-Si:H	a-Si:H	Metal oxides	Organic-TFT's
Drive capacity	High mobility, small W/L, pMOS,CMOS	Medium-high mobility, medium W/L, CMOS	Low mobility, large W/L, nMOS	Medium-high mobility, medium W/L, nMOS	Low mobility, large W/L, pMOS
Mobility [$cm^2V^{-1}s^{-1}$]	≥200	>100	≈1	>10	<5
V_T uniformity	poor	medium	good	Medium - good	poor
V_T variation	More stable than a-Si:H	More stable than a-Si:H	poor	More stable than a-Si:H ?	poor
I_{drive} uniformity	Poor – current programming	Poor – current programming	Poor – current programming	OK ?	poor
Leakage current	OK	OK	very good	OK	OK
Process technol.	PE-CVD, HW	PE-CVD or sputtering + recrystallization	PE-CVD, HW	Evap., printing	CVD, PVD
Process temp. [ºC]	150-300	>300	150-300	≤100	<200
Manufacturability Status	Small to medium area Very mature	Unknown (same equipment as a-Si:H) Lab scale	Small to very large area Very mature	Small to medium size area Maturing	Large area, large volume Starting
Cost / yield	High / medium	Medium / unknown	Low / high	Medium / medium	low ?? / unknown

Some issues & directions of research

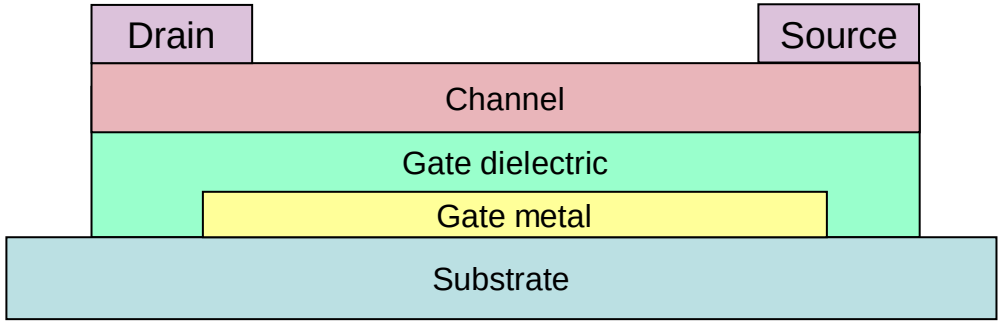
- Material issues
  - Higher mobility (poly-Si, LTPS, metal oxides, crystallization…)
  - Higher stability (crystalline semiconductors, new dielectrics,…)
  - Transparency (metal oxide,…)
  - Material selection (organics, metal oxides,…)
- Processing issues
  - Better uniformity (LTPS, complex circuits, …)
  - Scaling up
  - Flexible substrates
  - Low T processing (for polymeric substrates)
- Device issues
  - Higher pixel density (need higher mobility)
  - Higher integration
  - Flexible displays
  - All organic displays

Thin Film Silicon TFT configurations

Best configuration for optimum performance

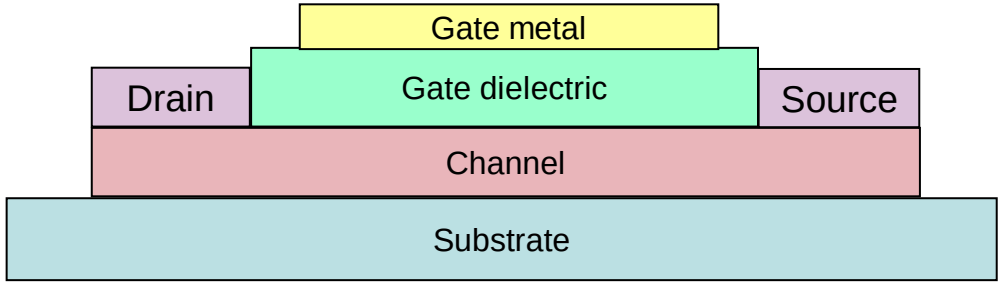
a-Si:H TFT

- Bottom gate
- Dielectric : Si_3N_4
- μ_{FET} ~ 0.5-1 cm^2/Vs

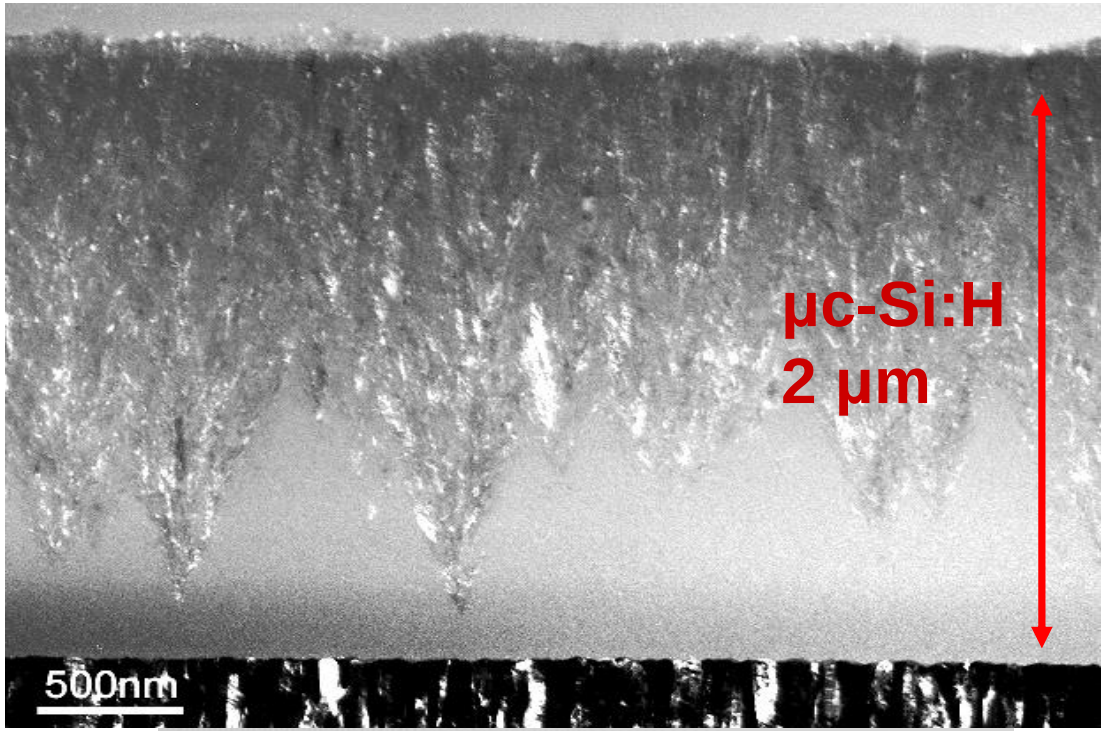


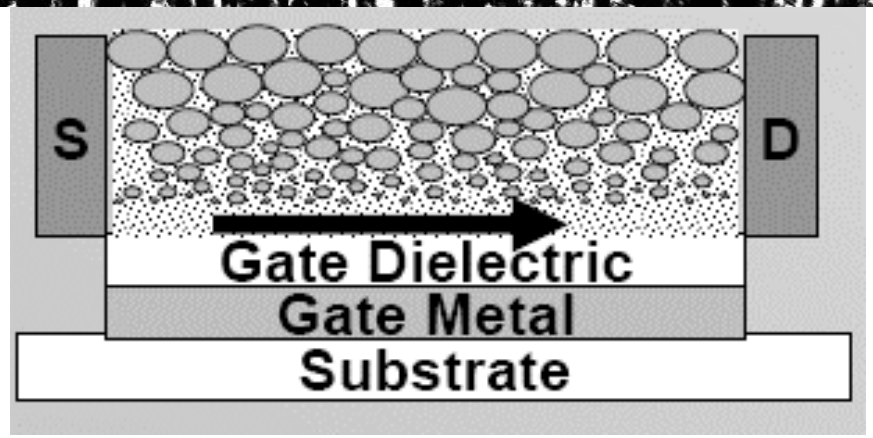
µc-Si:H, poly-Si

- Top gate
- Dielectric : SiO_2
- μ_{FET} ~ 3-500 cm^2/Vs



Growth of µc-Si:H, TFT configurations





- a-Si:H incubation phase usually present at the bottom of the layer
- Top gate µc-Si:H TFT insured better performance
- Bottom gate TFT more challenging
- Compatible with present a-Si:H TFT technology

Low T a-Si:H TFT's on plastic substrates

Process/Materials Challenges:

- Optimization of electronic material properties for electronic grade material ≤150ºC.

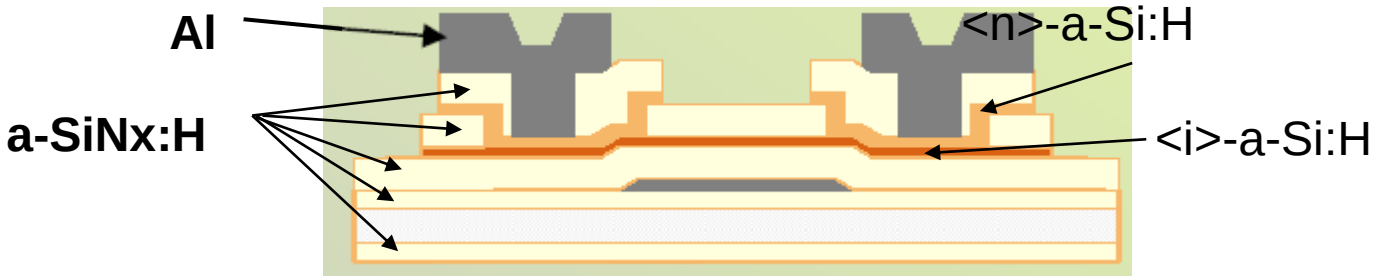
Issues:

- High defect density.
- High concentration of hydrogen
- Mechanical stress
- Dimensional stability of plastic substrates during processing
- Substrate handling

Process T [°C]	150	120	75	75 a-SiOx
Leakage [pA] (Dielectric quality)	<0.1	<1	<1	~1000
I_{on}/I_{off}	$>10^8$	$>10^6$	$>10^5$	$>10^3$
V_{th} [V] (Interface quality)	2.5	2.3	10	3
Slope [V/dec] (Interface quality)	0.3	0.5	2.1	1
μ_{FET} [cm^2/Vs] (Material quality)	1.2	0.8	0.03	~0.6

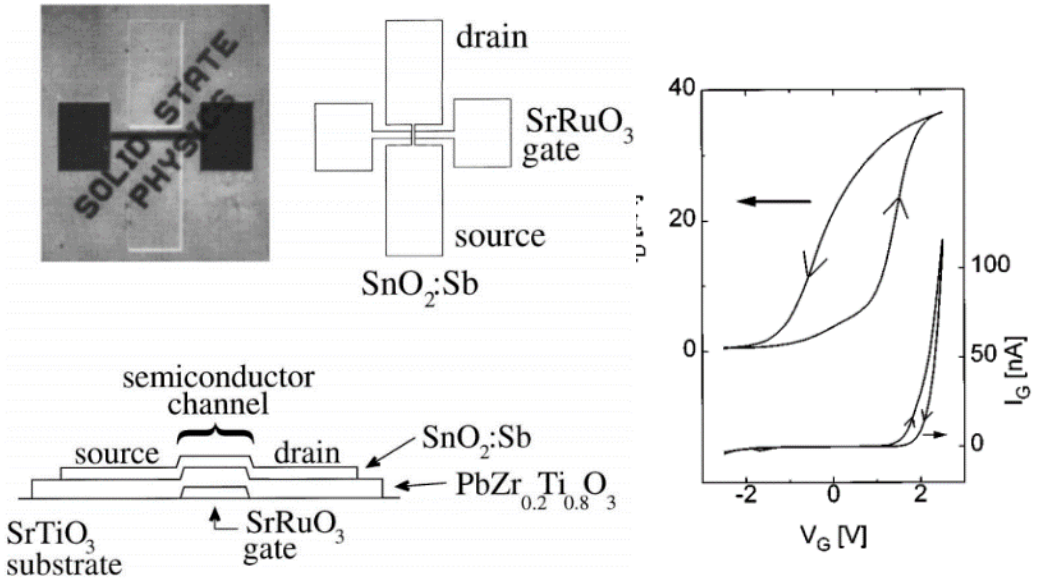
Dr. A. Sazonov, University of Waterloo, Ontario, Canada

Bottom gate

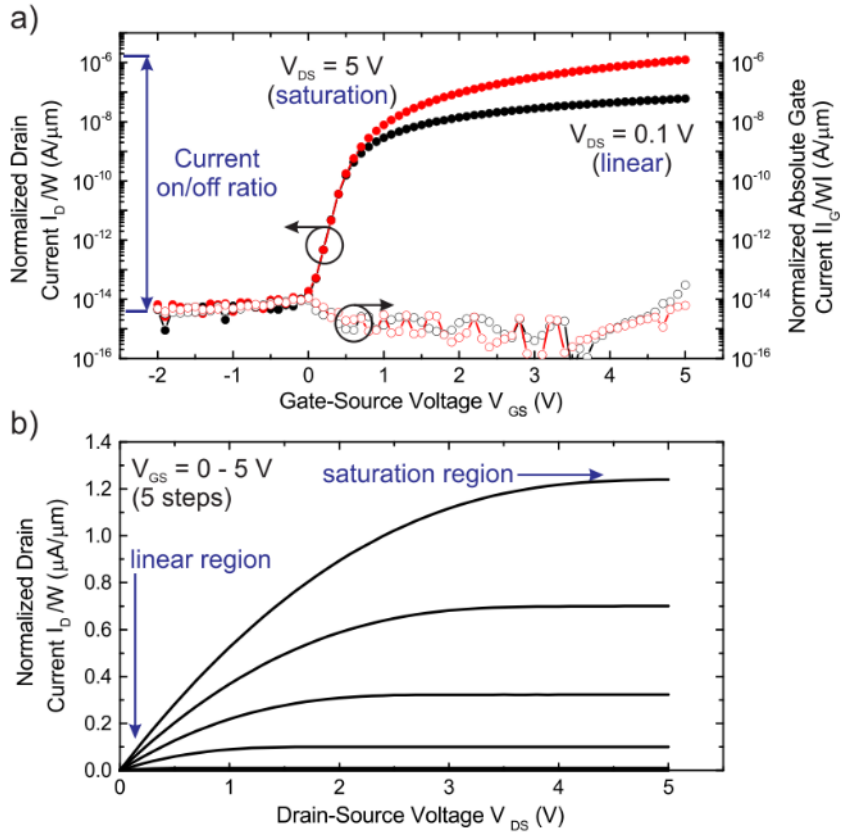


Metal oxide based TFT

- First metal oxide TFT
  (Prins et al, APL 1996)



- Recent developments based on IGZO (InGaZn Oxide)



Petti et al., Appl. Phys. Rev. 3, 021303 (2016)

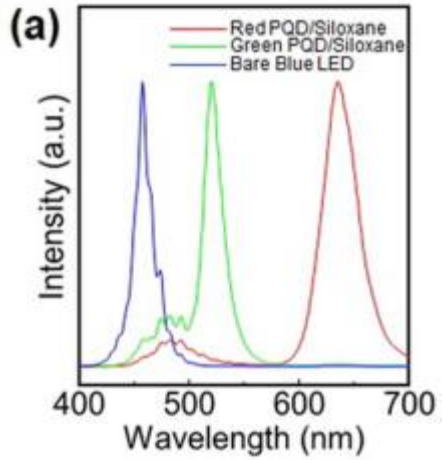
- LTPO (Low temperature poly oxide, IGZO) based displays in production (phones, tablets, TV,…)
- For example, iPhone 13 Pro, Samsung S21 Ultra

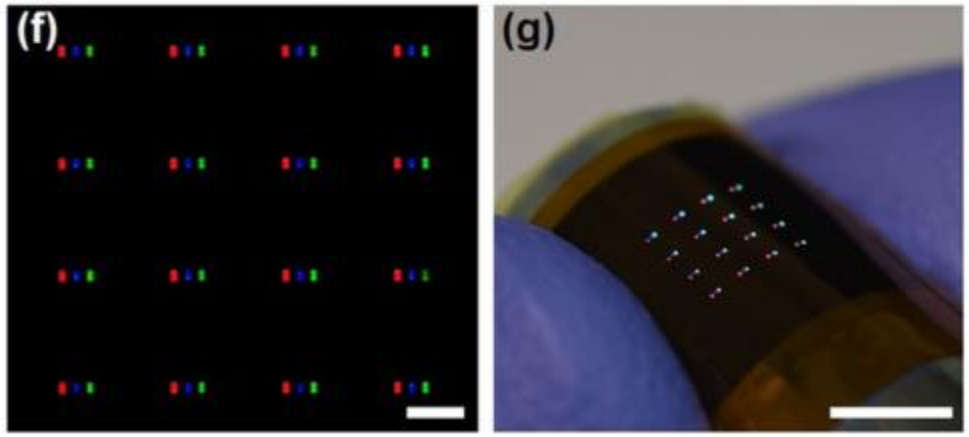
Advantages /disadvantages of IGZO

- Natural transparency
  - Less photosensitivity
- Better μ_{FET}
  - 30-50 > than a-SiH
  - Similar to LTPS
  - Suitable for high density displays
  - More efficient backlighting
- Low leakage current
  - Lower than LTPS
  - Lower display consumption
- More sensitive to failure due oxygen reactivity
  - Lower uniformity of μ
- Manufacturing challenges
  - Use of rare-earth metals (In, Ga)
  - Deposition

Perovskite LED for AM displays

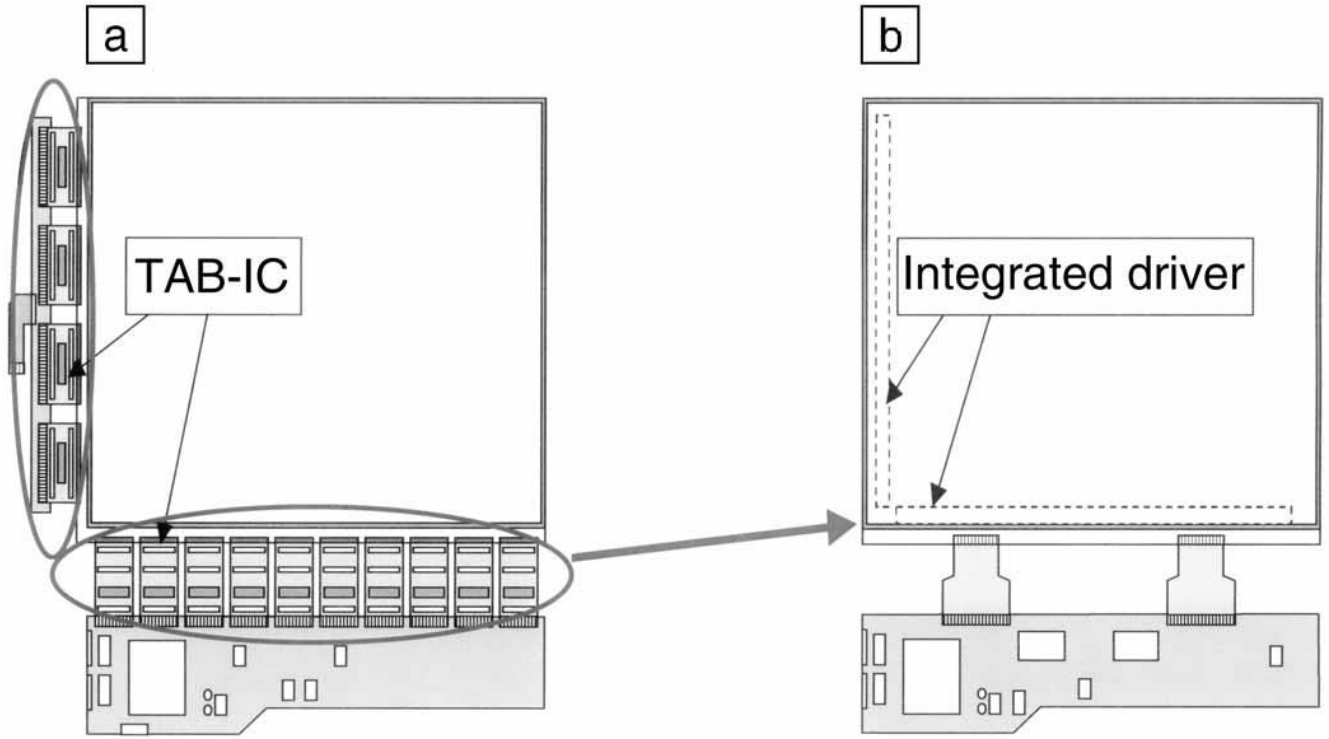
- Replace organic materials with perovskite LED in AMOLED displays
- Better lifetime





Hyung Cheoul Shim et al., Sci. Rep. 13 (2023)

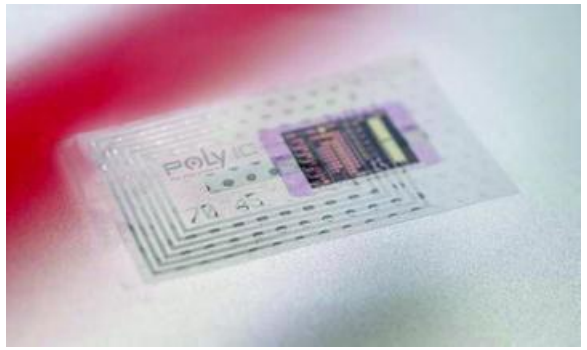
System integration

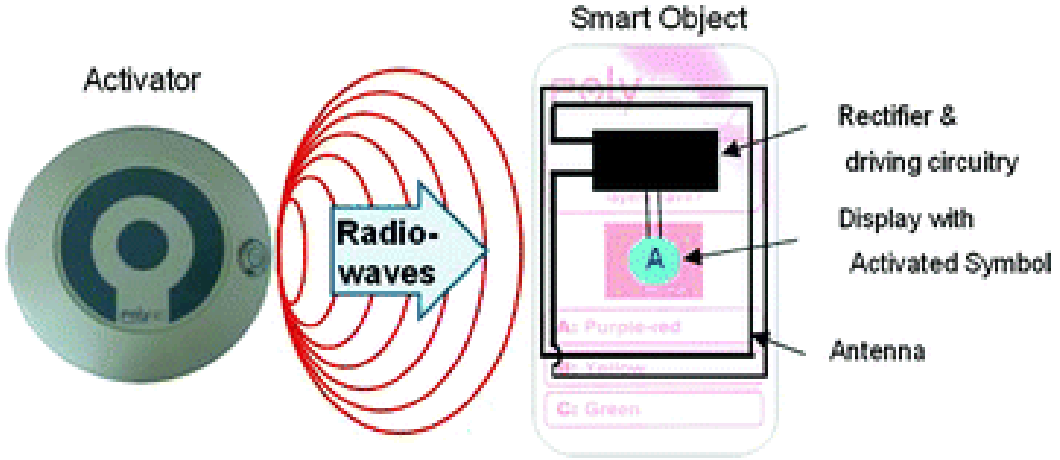


S. Uchikoga, MRS Bulletin 2002

- Long term prospect: System on display (SOD), entire PC on same substrate
- Printed electronic (mainly organic materials)

Printed electronics

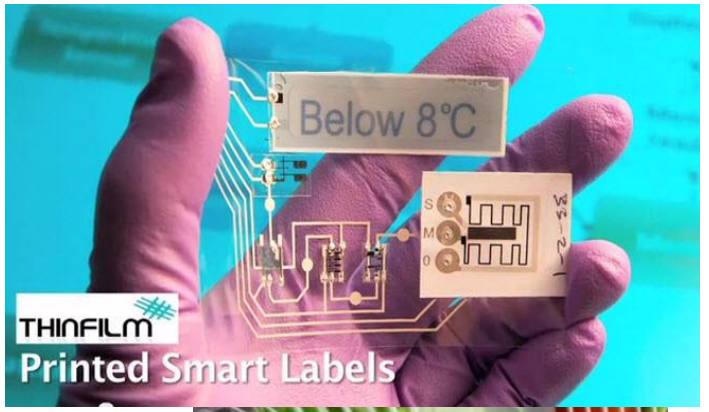




Brand protection

Electronic vouchers with printed RFID

Packaging monitoring



PolyIC, W. Clemens et al, in Organic and Printed Electronics (2012)

Bibliography

- Books
  - S.M. Sze, Semiconductor Devices
  - J. Kanicki, Amorphous and Microcrystalline Semiconductor Devices, 1991, Artech House
  - R.A. Street, Hydrogenated Amorphous Silicon, 1991, Cambridge University Press
  - Y. Kuo, “Thin film transistors, Materials and Processes”, Vol. 1, 2004, Kluwer Academic Publishers
  - J. Kanicki and J. Martin, “Hydrogenated amorphous silicon thin-film transistors”, in “Thin-Film Transistors”, 2003, Marcel Dekker Inc, chapter by http://www.eecs.umich.edu/omelab/downloads
- Papers
  - L. Petti et al., Appl. Phys. Rev. 3, 021303 (2016)
  - http://www.androidauthority.com/amorphous-igzo-and-beyond-399778/